

# Intel<sup>®</sup> Server System R2000IP Product Family

# **Technical Product Specification**

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**Enterprise Platforms and Services Division** 

# **Revision History**

| Date     | Revision Number | Modifications    |
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| May 2012 | 1.0             | Initial release. |

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# 1. Introduction

This Technical Product Specification (TPS) provides system level information for the Intel<sup>®</sup> Server System R2000IP product families. The system level features of both these product families are common, however the server board integrated into them is different. The Intel<sup>®</sup> Server System R2000IP product family is integrated with an Intel<sup>®</sup> Server Board S2600IP.

This document will describe the functions and features of the integrated server system which includes the chassis layout, system boards, power sub-system, cooling sub-system, and storage sub-system options. Server board specific detail can be obtained by referencing the Intel® Server Board S2600IP Technical Product Specification.

In addition, design-level information related to specific server board components/subsystems can be obtained by ordering External Product Specifications (EPS) or External Design Specifications (EDS) related to this server generation. EPS and EDS documents are made available under NDA with Intel and must be ordered through your local Intel representative. See the Reference Documents section at the end of this document for a complete list of available documents.

# 1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 Introduction
- Chapter 2 Product Family Overview
- Chapter 3 Power Subsystem
- Chapter 4 Thermal and Acoustic Management
- Chapter 5 System Storage and Peripheral Drive Bays
- Chapter 6 Front Control Panel and I/O Panel Overview
- Appendix A Integration and Usage Tips
- Glossary
- Reference Documents

#### 1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel® ensures through its own chassis development and testing that when Intel® server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel®-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

# 2. Product Family Overview

The Intel® Server System R2000IP is rack mount 2U server systems. This generation of Intel® 2U server platforms offers a variety of system options to meet the varied configuration requirements of high-density high-performance computing environments.

This chapter provides a high-level overview of the system features and available platform options as offered in different platform SKUs. Greater detail for each major system component or feature is provided in the following chapters.

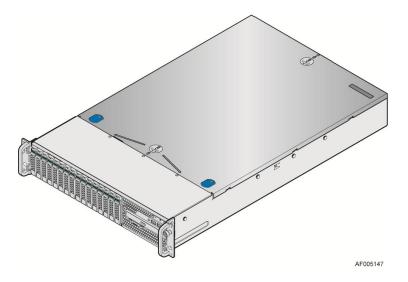


Figure 1. System Overview

**Note**: The following table lists features. Features that are unique to one product family will be identified by either denoting the server system name or the integrated server board name.

**Table 1. System Feature Set** 

| Feature                        | Description   |  |
|--------------------------------|---|--|
| Processor Support              | <ul> <li>Support for one or two Intel<sup>®</sup> Xeon<sup>®</sup> processors E5-2600 product family with a Thermal Design<br/>Power (TDP) of up to 135 W.</li> </ul> |  |
|                                | ■ 16 DIMM slots – 2 DIMMs/Channel – 4 memory channels per processor   |  |
|                                | <ul> <li>Unbuffered DDR3 and registered DDR3 DIMMs</li> </ul>   |  |
| Memory                         | <ul><li>Memory DDR3 data transfer rates of 800, 1066, 1333 MT/s and 1600 MT/s</li></ul>   |  |
|                                | <ul> <li>DDR3 standard I/O voltage of 1.5V and DDR3 Low Voltage of 1.35V</li> </ul>   |  |
| Chipset                        | Intel® C600-A chipset with support for optional Storage Option Select keys  |  |
|                                | ■ Video – Back Panel  |  |
| External I/O                   | Serial Port   |  |
| connections                    | <ul> <li>Four RJ-45 Network Interface Connectors supporting 10/100/1000Mb</li> </ul>  |  |
|                                | ■ Four USB 2.0 Port + 2 on front panel on non-max hard drive SKUs   |  |
| Internal I/O                   | ■ Two Type-A USB 2.0 connector  |  |
| connectors/headers             | ■ One DH-10 Serial-B port connector   |  |
| Optional I/O Module<br>Support |   |  |

| System Fans  | Six managed system fans   |  |
|--|---|--|
| System Fans  | One power supply fan for each installed power supply module                                   |  |
|  | ■ Eight (8) LP PCI cards without riser  |  |
| Expansion Slots  | 1 PCIe IO module connector  |  |
|  | ■ 1 PCIe SAS Module connector   |  |
| Video  | ■ Integrated 2D Video Controller  |  |
|  | One low-profile eUSB 2x5 pin connector to support low-profile eUSB solid state devices        |  |
|  | ■ Two single port SATA connectors capable of supporting up to 6 GB/sec                        |  |
| On-board storage controllers and options                   | ■ Two 4-port mini-SAS connectors capable of supporting up to 3 GB/sec SAS/SATA                |  |
| controllers and options                                    | ■ Intel SAS ROC module support (Optional)   |  |
|  | ■ Intel® RAID C600 Upgrade Key support providing optional expanded SATA/SAS RAID capabilities |  |
| Security   | Trusted Platform Module (Optional)  |  |
|  | ■ Integrated Baseboard Management Controller, IPMI 2.0 compliant                              |  |
| O  | ■ Support for Intel <sup>®</sup> Server Management Software                                   |  |
| Server Management  | ■ Intel <sup>®</sup> Remote Management Module 4 support (Optional)                            |  |
|  | ■ Intel® Remote Management Module 4 Lite support (Optional)                                   |  |
| Power Supply Options • 750W (1+1,1+0,2+0) Hot-swap Capable |   |  |
|  | ■ 8x – 3.5" SATA/SAS Hot Swap Hard Drive Bays + Optical Drive support                         |  |
|  | ■ 12x – 3.5" SATA/SAS Hot Swap Hard Drive Bays  |  |
| Storage Bay Options  | ■ 8x – 2.5" SATA/SAS Hot Swap Hard Drive Bays + Optical Drive support                         |  |
|  | ■ 16x – 2.5" SATA/SAS Hot Swap Hard Drive Bays + Optical Drive support                        |  |
|  | ■ 24x – 2.5" SATA/SAS Hot Swap Hard Drive Bays  |  |
|  | ■ Tool-less rack mount rail kit   |  |
| Dook Mount Kit Ontions                                     | Value rack mount rail kit   |  |
| Rack Mount Kit Options                                     | Cable Management Arm  |  |
|  | 2-post Fixed mount bracket kit  |  |

# 2.1 System Dimensions

**Table 2. Dimensional Data** 

|                                   | Std inches | Metric - mm   |
|-----------------------------------|------------|---------------|
| Height                            | 3.34       | 87.63         |
| Width without rails               | 17.244     | 438.0         |
| Width with rails                  | 17.716     | 450.0         |
| Depth without CMA*                | 32.0       | 812.8         |
| Depth with CMA                    | 35.0       | 889.0         |
| Maximum Weight (Fully Integrated) | 52 lbs     | 23.6 Kg (ref) |

<sup>\*</sup>Cable Management Arm

# 2.2 System Level Environmental Limits

The following table defines the Intel<sup>®</sup> Server System R2000IP system level operating and non-operating environmental limits. Operation of the Intel<sup>®</sup> Server System R2000IP at conditions beyond those shown in the following table may cause permanent damage to the system. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

**Table 3. System Environmental Limits Summary** 

| Parameter                               |  | Limits  |  |
|---|--|---|--|
| Temperature                             |  |   |  |
|   | Operating                                | ASHRAE Class A2 – Continuous Operation. 10° C to 35° C (50° F to 95° F) with the maximum rate of change not to exceed 10°C per hour |  |
|   |  | ASHRAE Class A3 – Includes operation up to 40C for up to 900 hrs per year.  |  |
|   |  | ASHRAE Class A4 – Includes operation up to 45C for up to 90 hrs per year.   |  |
|   | Shipping                                 | -40° C to 70° C (-40° F to 158° F)  |  |
| Altitude                                |  |   |  |
|   | Operating                                | Support operation up to 3050m with ASHRAE class deratings.  |  |
| Humidity                                |  |   |  |
|   | Shipping                                 | 50% to 90%, non-condensing with a maximum wet bulb of 28° C (at temperatures from 25° C to 35° C)                                   |  |
| Shock                                   |  |   |  |
|   | Operating                                | Half sine, 2g, 11 mSec  |  |
|   | Unpackaged                               | Trapezoidal, 25 g, velocity change is based on packaged weight  |  |
|   | Packaged                                 | Product Weight: ≥ 40 to < 80  |  |
|   |  | Non-palletized Free Fall Height = 18 inches Palletized (single product) Free Fall Height = NA                                       |  |
| Vibration                               |  |   |  |
|   | Unpackaged                               | 5 Hz to 500 Hz 2.20 g RMS random  |  |
|   | Packaged                                 | 5 Hz to 500 Hz 1.09 g RMS random  |  |
| AC-DC                                   |  |   |  |
|   | Voltage                                  | 90 Hz to 132 V and 180 V to 264 V   |  |
|   | Frequency                                | 47 Hz to 63 Hz  |  |
|   | Source<br>Interrupt                      | No loss of data for power line drop-out of 12 mSec  |  |
|   | Surge Non-<br>operating and<br>operating | Unidirectional  |  |
|   | Line to earth                            | AC Leads 2.0 kV   |  |
|   | Only                                     | I/O Leads 1.0 kV  |  |
| FCD                                     |  | DC Leads 0.5 kV   |  |
| ESD                                     | Δ:-                                      | 42.0 lb/  |  |
|   | Air<br>Discharged                        | 12.0 kV   |  |
|   | Contact<br>Discharge                     | 8.0 kV  |  |
| Acoustics<br>Sound<br>Power<br>Measured |  |   |  |
|   | Power in<br>Watts                        | <300 W ≥300 W ≥600 W ≥1000 W  |  |
|   | Servers/Rack<br>Mount BA                 | 7.0 7.0 7.0 7.0   |  |
|   |  |   |  |

Note:

Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel<sup>®</sup> server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel<sup>®</sup> developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

**Disclaimer Note**: Intel® ensures the unpackaged server board and system meet the shock requirement mentioned above through its own chassis development and system configuration. It is the responsibility of the system integrator to determine the proper shock level of the board and system if the system integrator chooses different system configuration or different chassis. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of its published operating or non-operating limits.

# 2.3 System Features and Options Overview

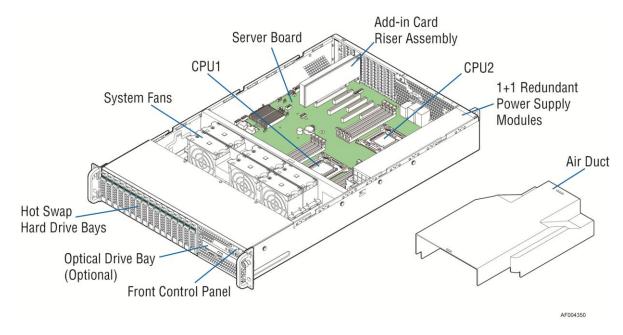


Figure 2. System Components Overview

# 2.3.1 Hot Swap Hard Drive Bay and Front Panel Options

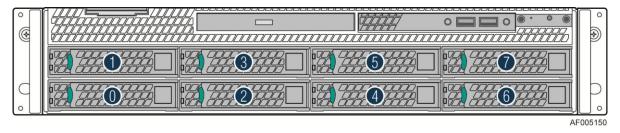


Figure 3. 3.5" Hard Drive Bay - 8 Drive Configuration

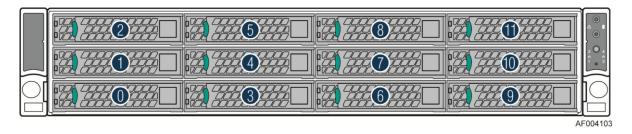


Figure 4. 3.5" Hard Drive Bay - 12 Drive Configuration

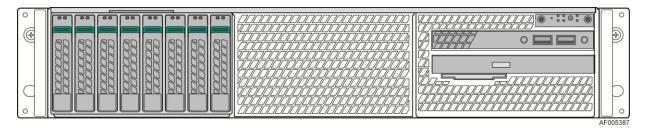


Figure 5. 2.5" Hard Drive Bay - 8 Drive Configuration

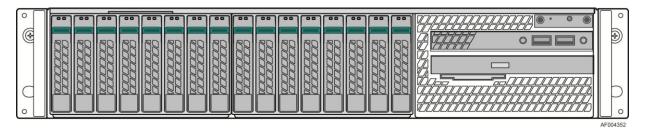


Figure 6. 2.5" Hard Drive Bay - 16 Drive Configuration

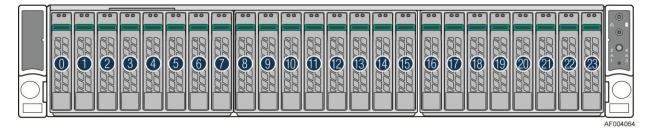


Figure 7. 2.5" Hard Drive Bay - 24 Drive Configuration

## 2.3.2 Back Panel Features

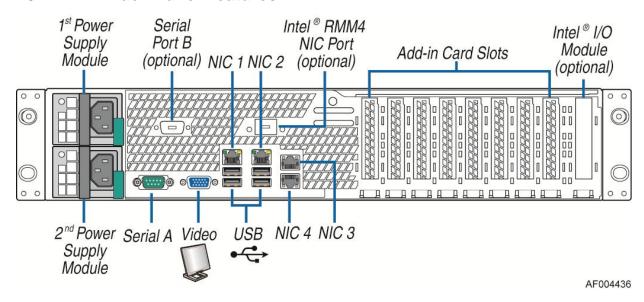
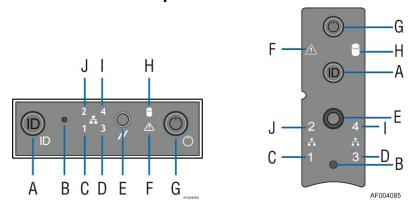


Figure 8. Back Panel Feature Identification

# 2.3.3 Front Control Panel Options



| Label | Description                                  |   | Description                   |
|-------|--|---|-------------------------------|
| Α     | System ID Button w/Integrated LED            | F | System Status LED             |
| В     | NMI Button (recessed, tool required for use) | G | Power Button w/Integrated LED |
| С     | NIC-1 Activity LED                           | Н | Hard Drive Activity LED       |
| D     | NIC-3 Activity LED                           | I | NIC-4 Activity LED            |
| Е     | System Cold Reset Button                     | J | NIC-2 Activity LED            |

**Figure 9. Front Control Panel Options** 

#### 2.4 Server Board Features Overview

The following illustration provides a general overview of the server board, identifying key feature and component locations. The accompanying table will identify variations when present.

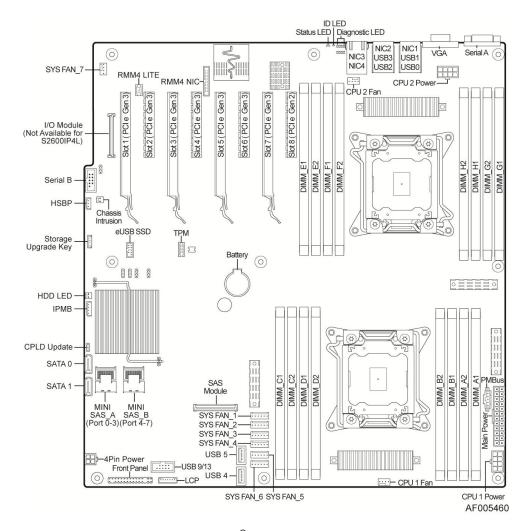


Figure 10. Intel® Server Board S2600IP

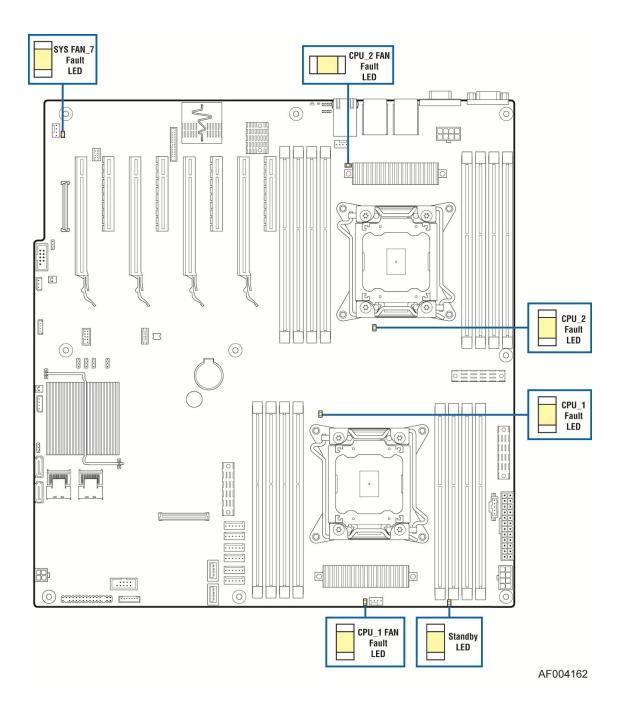


Figure 11. Stand by LED, Fan Fault LED and CPU Fault LED Location

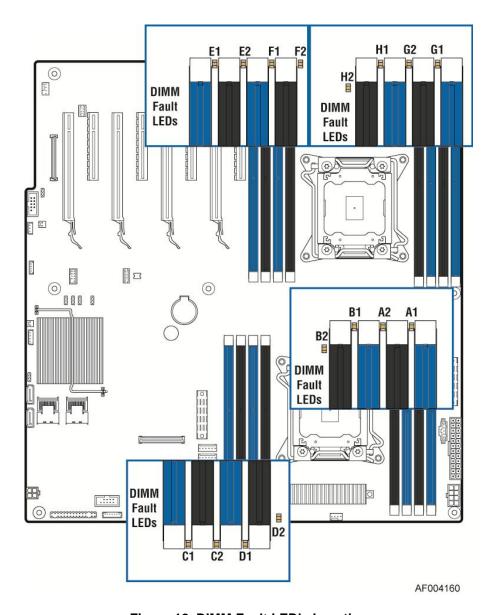


Figure 12. DIMM Fault LED's Location

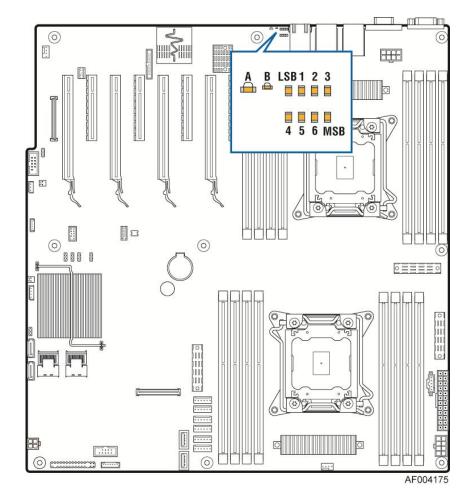


Figure 13. Location of System Status, System ID and POST Code Diagnostic LEDs

| LED Name            | Description               |  |
|---------------------|---------------------------|--|
| Α                   | System Status LED         |  |
| В                   | System ID LED             |  |
| LSB 1 2 3 4 5 6 MSB | Post Code Diagnostic LEDs |  |

# 2.5 Front Bezel Support

The optional front bezel is made of molded plastic and uses a snap-on design. When installed, its design allows for maximum airflow to maintain system cooling requirements. The bezel assembly includes snap-in options that can be used for customization.

(Intel Product Order Code – A2UBEZEL)



Figure 14. Optional Front Bezel

# 2.6 Available Rack and Cabinet Mounting Kit Options

- Tool-less rack mount rail kit Intel Product Code AXXPRAIL
  - o 1U and 2U compatible
  - o 65 lbs max support weight
  - Tool-less installation
  - Full extension from rack
  - Drop in system install
  - Optional cable management arm support
- Value rack mount rail kit Intel Product Code AXXVRAIL
  - 1U to 4U compatible
  - 130 lbs max support weight
  - Tool-less chassis attach
  - o Tools required to attach to rails to rack
  - 2/3 extension from rack
- Cable Management Arm Intel Product Code AXX1U2UCMA (\*supported with AXXPRAIL only)
- 2-Post Fixed mount bracket kit Intel Product Code AXX2POSTBRCKT

# 3. Power Subsystem

There is 750 Watt AC power supply module available. This chapter will provide the power supply specification details.

The power supply will accept a wide input voltage range of 90 to 264Vac, while providing precisely regulated 12Vdc output voltage at 750W. The power supply will encompass all protective features and conform to safety agency regulatory requirements. The power will be designed for redundant operation and includes an active OR'ing circuit for isolation. PMBus\* communications protocol will be included to interface with external devices for communication.

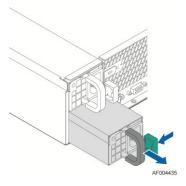


Figure 15. 750w Power Supply

#### 3.1 Mechanical Overview

The physical size of the power supply enclosure is 40.25mm x 54.5mm x 320mm (H x W x D). The 1+1 configuration of 750W power supply enclosure dimensional drawing is shown below:

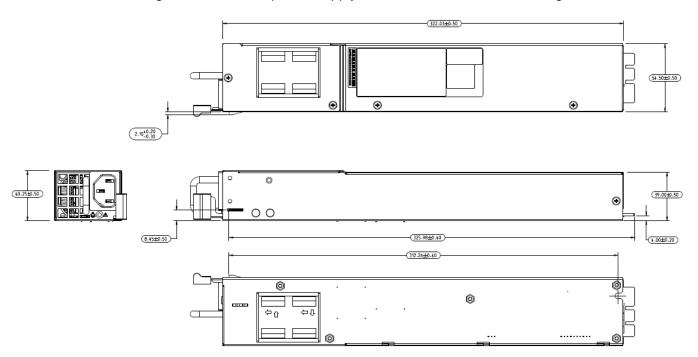
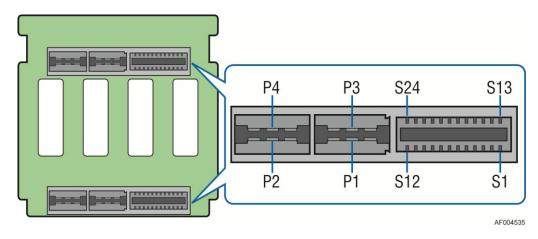


Figure 16. Power Supply Module Mechanical Drawing

# 3.2 Power Distribution Board and Power Interface board

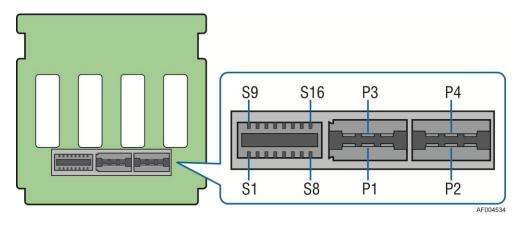
# 3.2.1 Input Connectors to Power Interface board (PSU mating connectors)



| Pin | Signal                      | Pin | Signal             |  |
|-----|-----------------------------|-----|--------------------|--|
| S1  | +12V Remote Sense           | S13 | n.c.               |  |
| S2  | +12V Remote Sense<br>Return | S14 | n.c.               |  |
| S3  | 12V Load Share              | S15 | A0                 |  |
| S4  | SMBAlert#                   | S16 | Present (not used) |  |
| S5  | SDA                         | S17 | Vbias (not used)   |  |
| S6  | SCL                         | S18 | n.c.               |  |
| S7  | PSKILL (grounded)           | S19 | n.c.               |  |
| S8  | PSON                        | S20 | n.c.               |  |
| S9  | PWOK                        | S21 | n.c.               |  |
| S10 | A1                          | S22 | n.c.               |  |
| S11 | 5VSB                        | S23 | 5VSB               |  |
| S12 | 5VSB                        | S24 | 5VSB               |  |
| P1  | +12V output                 | P3  | Ground             |  |
| P2  | +12V output                 | P4  | Ground             |  |

Figure 17. Power Supply Interface Connector Pin-out on Interface Board

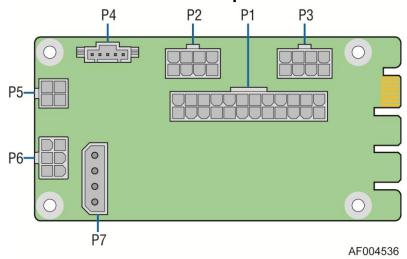
# 3.2.2 Connector from Interface Board to power distribution board



| Pin | Signal                      | Pin | Signal           |
|-----|-----------------------------|-----|------------------|
| S1  | +12V Remote Sense           | S9  | 5VSB             |
| S2  | +12V Remote Sense<br>Return | S10 | 5VSB             |
| S3  | SMBAlert#                   | S11 | Vbias (not used) |
| S4  | SDA                         | S12 | 5VSB             |
| S5  | SCL                         | S13 | 5VSB             |
| S6  | PSON                        | S14 | n.c.             |
| S7  | PWOK 1                      | S15 | n.c.             |
| S8  | PWOK 2                      | S16 | n.c.             |
| P1  | +12V output                 | P3  | Ground           |
| P2  | +12V output                 | P4  | Ground           |

Figure 18. Power Distribution Board Interface Connector Pin-out on Interface Board

# 3.2.3 Power Distribution Board Output Connectors



| Connector                                | No. of pins               | Description                            |  |  |
|--|---------------------------|--|--|--|
| P1                                       | 24                        | Motherboard Main Power Connector       |  |  |
| P2                                       | 8                         | CPU1 Power Connector                   |  |  |
| P3                                       | 8                         | CPU2 Power Connector                   |  |  |
| P4                                       | 5                         | PMBus* Connector                       |  |  |
| P5 4 Motherboard 2x2 12V power connector |                           | Motherboard 2x2 12V power connector    |  |  |
| P6                                       | P6 6 HSBP power connector |  |  |  |
| P7                                       | 4                         | Peripherals Power connector (CD, SSDs) |  |  |

Figure 19. Power Distribution Board Output Connectors

#### 3.2.3.1 Power Distribution Board Connectors Pin definition

Table 4. P1 Baseboard Power Connector (P1)

| Pin | Signal  | Pin | Signal   |
|-----|---------|-----|----------|
| 1   | +3.3VDC | 13  | +3.3VDC  |
| 2   | +3.3VDC | 14  | -12VDC   |
| 3   | COM     | 15  | COM      |
| 4   | +5VDC   | 16  | PSON#    |
| 5   | COM     | 17  | СОМ      |
| 6   | +5VDC   | 18  | COM      |
| 7   | COM     | 19  | COM      |
| 8   | PWR OK  | 20  | Reserved |
| 9   | 5 VSB   | 21  | +5VDC    |
| 10  | +12V1   | 22  | +5VDC    |
| 11  | +12V1   | 23  | +5VDC    |
| 12  | +3.3VDC | 24  | COM      |

Table 5. Processor Power Connectors (P2, P3)

| Pin | Signal | 18 AWG color | Pin | Signal | 18 AWG Color |  |
|-----|--------|--------------|-----|--------|--------------|--|
| 1   | COM    | Black        | 5   | +12V1  | Yellow       |  |
| 2   | COM    | Black        | 6   | +12V1  | Yellow       |  |
| 3   | СОМ    | Black        | 7   | +12V1  | Yellow       |  |
| 4   | COM    | Black        | 8   | +12V1  | Yellow       |  |

Table 6. PMBus\* (P4)

| Pin | Signal    | 24 AWG Color |
|-----|-----------|--------------|
| 1   | I2C Clock | White        |
| 2   | I2C Data  | Yellow       |
| 3   | SMBAlert# | Red          |
| 4   | СОМ       | Black        |
| 5   | 3.3RS     | Orange       |

Table 7. 2x2 pin 12V Power Connectors (P5)

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1   | COM    | 3   | +12V1  |
| 2   | COM    | 4   | +12V1  |

**Table 8. HSBP Power Connectors (P6)** 

| Pin | Signal | Pin | Signal        |
|-----|--------|-----|---------------|
| 1   | COM    | 4   | +12V2 (240VA) |
| 2   | COM    | 5   | +12V3 (240VA) |
| 3   | COM    | 6   | +12V3 (240VA) |

**Table 9. Peripheral Power Connector (P7)** 

| Pin | Signal | 18 AWG Color |
|-----|--------|--------------|
| 1   | +12V1  | Yellow       |
| 2   | COM    | Black        |
| 3   | COM    | Black        |
| 4   | +5 VDC | Red          |

## 3.3 Power Supply Module Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels: 100%, 50% and 20%. Efficiency is tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 10. 750W Power supply efficiency

| AC Input   | 115VAC       |     |     | 2   | 230VAC |     |
|------------|--------------|-----|-----|-----|--------|-----|
| Load       | 20% 50% 100% |     | 20% | 50% | 100%   |     |
| Efficiency | 87%          | 90% | 87% | 88% | 92%    | 88% |

Note: Fan power is supplied by an external power supply when efficiency is measured.

# 3.4 AC Power Cord Specification Requirements

The AC power cord used must meet the specification requirements listed in the following table.

**Table 11. AC Power Cord Specifications** 

| Cable Type         | SJT    |
|--------------------|--------|
| Wire Size          | 16 AWG |
| Temperature Rating | 105°C  |
| Amperage Rating    | 13 A   |
| Voltage Rating     | 125 V  |

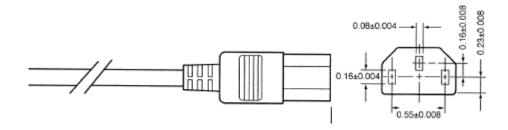


Figure 20. AC Power Cord

# 3.5 AC Input Requirement

The power supply shall incorporate universal power input with active power factor correction which shall reduce line harmonics in accordance with the EN61000-3-2 and JEIDA MITI standards.

#### 3.5.1 AC Inlet Connector

The AC input connector shall be an *IEC 320 C-14* power inlet. This inlet is rated for 15A/250VAC.

#### 3.5.2 AC Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage range, shown in below table. Harmonic distortion of up to 10% of rated AC Input Voltage must not cause the power supply to go out of specified limits. The power supply shall power off on or after/below 75Vac ±5Vac range. The power supply shall start up on or before/above 85VAC ±4Vac. Application of an input voltage below 85VAC shall not cause damage to the power supply, including a fuse blow.

| Parameter                | MIN         | RATED       | MAX     | Start-up<br>Vac | Power Off<br>Vac | Max Input AC<br>Current | Max Rated Input AC<br>Current |
|--------------------------|-------------|-------------|---------|-----------------|------------------|-------------------------|-------------------------------|
| Line Voltage<br>(110VAC) | 90Vrm<br>s  | 100-127Vrms | 140Vrms | 85Vac<br>±4Vac  | 75Vac<br>±5Vac   | 10.0 Arms 1,3           | 9.0 Arms 4                    |
| Line Voltage<br>(220VAC) | 180Vr<br>ms | 200-240Vrms | 264Vrms | 85Vac<br>±4Vac  | 75Vac<br>±5Vac   | 6.0 Arms 2,3            | 5.0 Arms 4                    |
| Frequency                | 47 Hz       | 50/60Hz     | 63 Hz   |                 |                  |                         |                               |

Table 12. AC Input Voltage Range

#### Notes:

- 1. Maximum input current at low input voltage range shall be measured at 90VAC, at max load.
- 2. Maximum input current at high input voltage range shall be measured at 180VAC, at max load.
- 3. This requirement is not to be used for determining agency input current markings.
- 4. Maximum rated input current is measured at 100VAC and 200VAC

#### 3.5.3 Power Factor Correction

The power supply shall incorporate a Power Factor Correction circuit. The power supply shall be tested as described in EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits-Section 2: Limits for harmonic current emissions, and shall meet the harmonic current emissions limits specified for ITE equipment. The power supply shall be tested as described in JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment and shall meet the harmonic current emissions limits specified for ITE equipment.

#### 3.5.4 Power Recovery

The power supply will recover automatically after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

#### 3.5.5 Voltage Brown Out

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition the power supply shall meet the following:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout condition. Maximum input current under a continuous brownout shall not blow the fuse. The power supply should tolerate a 3min ramp from 90VAC voltage to 0VAC after the components have reached a steady state condition.

#### 3.5.6 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

#### 3.5.7 AC Line Dropout/Holdup

An AC line dropout is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout of 12ms or less the power supply must meet dynamic voltage regulation requirements over the rated load. An AC line dropout of 12ms or less shall not cause any tripping of control signals or protection circuits (= 12ms holdup time requirement). If the AC dropout lasts longer than 12ms, the power supply should recover and meet all turn-on requirements. The power supply must meet the AC dropout requirement over rated AC voltages, frequencies, and output loading conditions. Any dropout of the AC line shall not cause damage to the power supply.

# 3.5.8 AC Line 5VSB Holdup

The 5VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=5VSB holdup time) whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

#### 3.5.9 AC Line Fuse

The power supply shall have a single line fuse, on the Line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a slow blow type. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

#### 3.5.10 **AC Inrush**

The peak AC inrush current shall be less than **40A peak** for one-quarter of the AC cycle and less than the ratings of power supply's critical AC input components, including: input fuse, bulk caps, rectifiers, and surge limiting device. The power supply must meet the AC inrush current requirements for any rated AC voltage, during turn-on at any phase of AC voltage,

during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range Top, (includes hot and cold inrush). It is acceptable that AC line inrush current may reach up to **60A peak** for up to 1msec.

# 3.5.11 AC Line Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring Wave and AC Unidirectional wave with **2kV for line to Gnd and 1kV for line to line** per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition. The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

### 3.5.12 AC Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. "Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage. The power supply shall meet the requirements under the following AC line sag and surge conditions.

AC Line Sag (10sec interval between each sagging) **Duration** Sag **Operating AC Voltage** Line Frequency **Performance Criteria** No loss of function or Continuous 10% Nominal AC Voltage ranges 50/60Hz performance 0 to 1 AC No loss of function or 95% Nominal AC Voltage ranges 50/60Hz cycle performance Loss of function acceptable, >30% Nominal AC Voltage ranges 50/60Hz > 1 AC cycle self-recoverable

**Table 13. AC Line Sag Transient Performance** 

**Table 14. AC Line Surge Transient Performance** 

| AC Line Surge   |       |                                     |                |                                    |  |  |
|-----------------|-------|-------------------------------------|----------------|------------------------------------|--|--|
| Duration        | Surge | Operating AC Voltage                | Line Frequency | Performance Criteria               |  |  |
| Continuous      | 10%   | Nominal AC Voltages                 | 50/60Hz        | No loss of function or performance |  |  |
| 0 to ½ AC cycle | 30%   | Mid-point of nominal AC<br>Voltages | 50/60Hz        | No loss of function or performance |  |  |

# 3.5.13 AC Line Fast Transient (EFT) Specification

The power supply shall meet the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5:1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot
  and undershoot, nor must it cause any nuisance trips of any of the power supply protection
  circuits.
- The surge-withstand test must not produce damage to the power supply.

<sup>\*</sup> Note: The load for a full cycle drop out will not exceed 360W.

The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

#### 3.5.14 AC Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, we can provide written confirmation of dielectric withstand test which includes: voltage level, duration of test and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

# 3.5.15 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification. For further information on Intel standards please request a copy of the Intel® Environmental Standards Handbook.

Table 15. Performance Criteria

| Level | Description   |
|-------|---|
| Α     | The apparatus shall continue to operate as intended. No degradation of performance.                       |
| В     | The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.    |
| С     | Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the |
|       | operation of the controls.  |

## 3.5.16 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

#### 3.5.17 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-4:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

# 3.5.18 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

#### 3.5.19 Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.

The pass criteria include: No unsafe operation is allowed under any condition; All power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

#### 3.5.20 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be not more than **1.75mA** when tested at 240VAC.

## 3.6 DC Output Requirement

#### 3.6.1 Connector

The power supply module shall use the card edge for output power to the power distribution board with **the mating connector of (Molex 459840005)** and AC input power to the module.

#### 3.6.2 Grounding

The ground of the pins of the power supply output connector provides the power return path. The output connector ground pins shall be connected to safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels, see section 7.11.

#### 3.6.3 Remote Sense

The power supply module uses remote sense (12VRS) to regulate out drops in the PDB connectors for the +12V output. The power supply has +12VRS- and +12VRS+ for remote sense to regulate out voltage drops for its +12V output voltage. The remote sense must be able to regulate out a minimum of 200mV drop.

#### 3.6.4 Output Power/Currents

These are the power requirements for the power supply module.

 750W

 Voltage
 Min
 Max
 Peak

 +12 V
 0.0 A
 62.5 A
 70.0 A<sup>1</sup>

 +5 VSB
 0.1 A
 3.0 A
 3.5 A<sup>1</sup>

**Table 16. Power Supply Module Load Ratings** 

Note: Peak current time duration doesn't exceed 12 sec

# 3.6.5 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. All outputs are measured with reference to the return remote sense signal (ReturnS). The +12V and +5Vsb voltages are measured at the PDB output harness connector.

**Table 17. Voltage Regulation Limits** 

| Output | Tolerance | MIN   | NOM   | MAX   | Units    |
|--------|-----------|-------|-------|-------|----------|
| + 12V  | ± 5%      | 11.40 | 12.00 | 12.60 | $V_{DC}$ |
| + 5Vsb | ± 5%      | 4.75  | 5.00  | 5.25  | $V_{DC}$ |

#### 3.6.6 5Vsb Outputs

The 5Vsb output shall be present when an AC input is greater than the power supply turn on voltage is applied.

#### 3.6.7 Fan Operation in Standby Mode

The power supply fans shall continue to operate at their lowest speed when in standby mode.

### 3.6.8 Dynamic Loading

The output voltages shall remain within limits specified in Table 10 for the step loading and capacitive loading. The load transient repetition rate shall be tested between 50Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The  $\Delta$  step load may occur anywhere within the MIN load to the MAX load shown in Voltage regulation Limits Table.

**Table 18. Transient Load Requirements** 

| Output | put Max ∆ Step Load Size Max Load Slew Rate |           | Test capacitive Load |  |
|--------|---|-----------|----------------------|--|
| +12V   | 40.0A                                       | 0.25 A/μs | 2000 μF              |  |
| +5VSB  | 0.5A*                                       | 0.25 A/μs | 20 μF                |  |

Note: Doesn't include fan transient.

# 3.6.9 Capacitive Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

**Table 19. Capacitive Loading Conditions** 

| Output | MIN  | MAX    | Units |
|--------|------|--------|-------|
| +12V   | 2000 | 11,000 | μF    |
| +5Vsb  | 20   | 350    | μF    |

# 3.6.10 Closed loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of **45 degrees phase margin** and **-10dB-gain margin** is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

#### 3.6.11 Common Mode Noise

The Common Mode noise on any output shall not exceed **350mV pk-pk** over the frequency band of 10Hz to 20MHz.

- 1. The measurement shall be made across a  $100\Omega$  resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure).
- 2. The test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

#### 3.6.12 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in table below. This is measured over a bandwidth of 0Hz to 20MHz at the power supply output connectors. A  $10\mu F$  tantalum capacitor in parallel with a  $0.1\mu F$  ceramic capacitor are placed at the point of measurement.

Table 20. Ripple and Noise

| Output       | +12V Output +5Vsb Output |         |
|--------------|--------------------------|---------|
| Ripple/Noise | 120mVp-p                 | 50mVp-p |

Note: When performing this test, the probe clips and capacitors should be located close to the load.

#### 3.6.13 Soft Starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified DC input or load conditions. There is no requirement for rise time on the 5Vstby but the turn on/off shall be monotonic.

#### 3.6.14 Zero Load Stability Requirements

When the power subsystem operates in a no load condition on all outputs including 5VSB in a 1+0 or 1+1 configuration, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

# 3.6.15 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The AC power will be disconnected from the power supply before the power supply is being extracted from the system. This could occur in standby mode or powered on mode. Insertion: The AC power will be connected to the power supply after the supply is inserted into the system and the supply will power on into standby mode or powered on mode.

In general, a failed (off by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

# 3.6.16 Timing Requirements

These are the timing requirements for the power supply operation. The 12V must rise from 10% to within regulation limits ( $T_{vout\_rise}$ ) within 5 to 70ms, 5Vsb - within 1.0 to 25ms. **Both outputs must rise monotonically**.

Table 21. Turn On/Off Timings

| Item                       | Description   | MIN | MAX  | Unit |
|----------------------------|---|-----|------|------|
| T <sub>sb_on_delay</sub>   | Delay from AC being applied to 5VSB being within regulation.  |     | 1500 | ms   |
| T <sub>5Vsb_rise</sub>     | 5Vsb Output voltage rise time   | 1.0 | 25   | ms   |
| T <sub>vout_rise</sub>     | DC Output voltage rise time   | 5.0 | 70   | ms   |
| T <sub>ac_on_delay</sub>   | Delay from AC being applied to DC output voltage being within regulation.                           |     | 2500 | ms   |
| $T_{vout\_holdup}$         | Time DC output voltage stay within regulation after loss of AC (See Section 6.8).                   | 13  |      | ms   |
| $T_{pwok\_holdup}$         | Delay from loss of AC to de-assertion of PWOK (See Section 6.8)                                     | 12  |      | ms   |
| T <sub>pson_on_delay</sub> | Delay from PSON <sup>#</sup> active to DC output voltage within regulation limits.                  | 5   | 400  | ms   |
| T <sub>pson_pwok</sub>     | Delay from PSON <sup>#</sup> de-active to PWOK being de-asserted.                                   |     | 50   | ms   |
| $T_{pwok\_on}$             | Delay from DC output voltage within regulation limits to PWOK asserted at turn on.                  | 100 | 500  | ms   |
| $T_{pwok\_off}$            | Delay from PWOK de-asserted to DC output voltage dropping out of regulation limits.                 | 1*  |      | ms   |
| $T_{pwok\_low}$            | Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal. | 100 |      | ms   |
| T <sub>sb_vout</sub>       | Delay from 5Vsb being in regulation to DC output voltage being in regulation at AC turn on.         | 50  | 1000 | ms   |
| T <sub>5VSB_holdup</sub>   | Time the 5Vsb output voltage stays within regulation after loss of AC.                              | 70  |      | ms   |
| T <sub>PSKil</sub>         | Delay from PSKILL= High to power supply turned off  |     | 100  | μS   |

#### Notes:

- 1. Must be tested at 1 full cycle dropout.
- 2. PSKill signal timing requirements may not be applicable as the PS module latch release requires removal of AC connector plug.

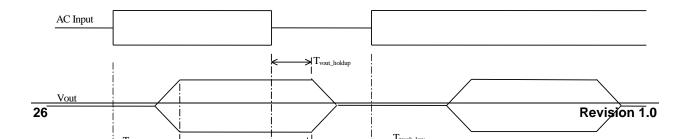


Figure 21. Turn On/Off Timing Diagram (Power Supply Signals)

#### 3.6.17 Residual Voltage Immunity in Standby Mode

The PS supply should be immune to any residual voltage placed on 12V output (typically a leakage voltage through the system from standby output) up to 500mV. This residual voltage shall not have any adverse effects on the PS, including: additional power dissipation or overstressing/over-heating any internal components or adversely affect the turn-on performance (no protection circuits tripping during turn on).

While in Stand-by mode, at no load condition, the residual voltage on 12V output shall not exceed 100mV.

#### 3.7 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON<sup>#</sup> cycle HIGH for 1sec shall be able to reset the power supply.

### 3.7.1 Over-current Protection (OCP)

The power supply shall have current limit to prevent the +12V, 5Vsb outputs from exceeding the values shown below. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON\* signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 5Vsb shall be protected under over-current or shorted conditions, so that no damage can occur to the power supply.

**Table 22. Over Current Protection Limits** 

| Output Voltage | OCP Limits |
|----------------|------------|

| +12V   | 70A min; 78A max  |
|--------|-------------------|
| + 5Vsb | 4.5Amin; 6.5A max |

The OCP limits should be provided in both redundant and non-redundant mode.

### 3.7.2 Over-voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON<sup>#</sup> signal or by an AC power interruption. The table below contains the over voltage limits. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Table 23. Over Voltage Protection (OVP) Limits

| Output Voltage | MIN (V) | MAX (V) |
|----------------|---------|---------|
| +12V           | 13.3    | 14.5    |
| + 5Vsb         | 5.7     | 6.5     |

#### 3.7.3 Over-temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PS module will shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 5Vsb remains always on. The OTP trip level shall have a minimum of 4°C of ambient temperature hysteresis, so that the power supply will not oscillate on and off due to temperature recovery condition. The power supply shall alert the system of the OTP condition from the power supply FAIL signal and the PWR LED.

#### 3.8 Control and Indicator Functions

The following sections define the input and output signals from the power supply. Signals that can be defined as low true use the following convention:  $signal^{\#} = low$  true.

#### 3.8.1 PSON# Input Signal

The PSON<sup>#</sup> signal is required to remotely turn on/off the power supply. PSON<sup>#</sup> is an active low signal that turns on the +12V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +5Vsb) turn off. This signal is pulled to +3.3V by a pull-up resistor internal to the power supply.

Table 24. PSON\* Signal Characteristic

| Signal Type             | Accepts an open collector/drain input from the system. Pull-up to +3.3V located in power supply. |
|-------------------------|--|
| PSON <sup>#</sup> = Low | ON   |

| PSON <sup>#</sup> = High or Open           | OFF   |        |
|--|-------|--------|
|  | MIN   | MAX    |
| Logic level low (power supply ON)          | 0V    | 0.4V   |
| Logic level high (power supply OFF)        | 2.4 V | 3.46 V |
| Source current, Vpson = low                |       | 2 mA   |
| Power up delay: T <sub>pson_on_delay</sub> | 5 ms  | 400 ms |
| PWOK delay: T <sub>pson pwok</sub>         |       | 50 ms  |

#### 3.8.2 **PSKILL**

The purpose of the PSKill pin is to allow for hot swapping of the power supply without arcing in the connector contacts. The PSKill pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKill pin will quickly turn off the power supply and prevent arcing of the DC output contacts. The DC output contacts must not arc under this condition. T<sub>PSKill</sub> (shown below in Table 16 PSKILL Signal Characteristics) is the minimum time delay from the PSKill pin unmating to when the power pins un-mate. The power supply must discharge its output inductor within this time from the un-mating of the PSKill pin. When the PSKill signal pin is not pulled down or left opened (power supply is extracting from the system), the power supply should shut down regardless of the condition of the PSON\* signal. The mating pin of this signal in the system should be tied to ground. Internal to the power supply, the PSKill pin should be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state signal at the PSKill pin, the power supply will be allowed to turn on by the PSON\* signal. A logic LOW on this pin by itself should not turn on the power outputs.

Signal Type (Input Signal to Supply) Accepts a ground input from the system. Pull-up to +3.3V located in the power supply. PSKILL = Low, PSON# = Low ON PSKILL = Open, PSON# = Low or Open OFF PSKILL = Low, PSON# = Open OFF MIN MAX Logic level low (power supply ON) 0V 0.4V 3.46V 2.4V Logic level high (power supply OFF) Source current, Vpskill = low 2mA Delay from PSKILL= High to power supply turned off 100μs (T<sub>PSKill</sub>)

**Table 25. PSKILL Signal Characteristics** 

T<sub>PSKill</sub> is the time from the PSKill signal de-asserting HIGH to the power supply's output inductor discharging.

**Note**: If PS module latch release would require removal of AC connector plug this signal is not necessary.

### 3.8.3 PWOK (Power OK) Output Signal

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

**Table 26. PWOK Signal Characteristics** 

| Signal Type                             | Open collector/drain output from power supply. Pull-up to +3.3V located in the power supply. |         |
|---|--|---------|
| PWOK = High                             | Power OK   |         |
| PWOK = Low                              | Power Not OK   |         |
|   | MIN  | MAX     |
| Logic level low voltage                 | 0V   | 0.4V    |
| Logic level high voltage                | 2.4 V  | 3.46 V  |
| Sink current, PWOK = low                |  | 400uA   |
| Source current, pull-up resistor        |  | 2mA     |
| PWOK delay: T <sub>pwok_on</sub>        | 100 ms   | 1000 ms |
| PWOK rise and fall time                 |  | 100 μs  |
| Power down delay: T <sub>pwok_off</sub> | 1 ms   | 200ms   |

### 3.8.4 A0, A1 Address Assignment Output Signal

A0 and A1 are dedicated to assignment the address for power supplies. See the table below for representation of the characteristics of A0 and A1.

Table 27. A0 and A1 Signal Characteristics

| Signal Type                      | Input, Pull-up to +3.3V located in power supply. |        |
|----------------------------------|--|--------|
|                                  | MIN  | MAX    |
| Logic level low voltage          | 0V   | 0.4V   |
| Logic level high voltage         | 2.4 V  | 3.46 V |
| Source current, pull-up resistor |  | 2mA    |

### 3.8.5 SCL and SDA Output Signals

SCL and SDA signals are tied to pull-up to +3.3V internal to the power supply with 49.9k resistors to prevent floating signals. Pull-up resistors are required on the system for proper operation.

**Table 28. SCL and SDA Signals Characteristics** 

| Signal Type                  | Open collector/drain output signal from power supply.  Pull-up to +3.3V located in system. |        |
|------------------------------|--|--------|
|                              | MIN  | MAX    |
| Logic level low voltage      | 0V   | 0.4V   |
| Logic level high voltage     | 2.4 V  | 3.46 V |
| Sink current Vout_low = 0.4V |  | 2mA    |

### 3.8.6 SMBALERT Output Signal

SMBALERT signal is open drain output signal to give an alert when any problem happens on PMBUS\*.

Table 29. SMBALERT Signal Characteristics

| Signal Type                  | Open Drain Output Signal, Low active |       |
|------------------------------|--------------------------------------|-------|
|                              | MIN                                  | MAX   |
| Logic level low voltage      | 0V                                   | 0.4V  |
| Logic level high voltage     |                                      | 3.46V |
| Sink current Vout_low = 0.4V |                                      | 2mA   |

#### 3.8.7 Power Supply Status LED

There will be a single bi-color LED to indicate power supply status. The LED operation is defined below.

**Table 30. LED Indicators** 

| Power Supply Condition   | LED state       |
|--|-----------------|
| No AC power to all power supplies  | OFF             |
| Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail, AC out of range, No AC power to this PSU only (for 1+1 configuration) | AMBER           |
| Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.                            | 1Hz Blink AMBER |
| AC present/Only 5VSB on (PS off)   | 1Hz Blink GREEN |
| Output ON and OK   | GREEN           |

The LEDs shall be visible on the power supply's exterior face. The LEDs' location shall meet ESD requirements. LEDs shall be securely mounted in such a way that incidental pressure on the LEDs shall not cause it to become displaced.

The LED shall be green or amber when lit. The LED shall be labeled with the two symbols below.

#### **Power Symbol**

Fail Symbol





### 3.8.8 12LS (Load Share) Signal

This input/output will allow two or more power supplies to share +12V output between them. The voltage of this signal will be a linear slope from zero to full load. The requirements below apply for both high line and low line condition. Whether operating on a high line or a low line, zero to 100% load as specified in section 7.4 will result in 0V to 8V on the current share line.

Table 31. Levels per load

| Total Load | Ishare<br>Minimum | Ishare Maximum | Number of supplies |
|------------|-------------------|----------------|--------------------|
| 100%       | 7.75V             | 8.25V          | 1                  |

| Total Load | Ishare<br>Minimum | Ishare Maximum | Number of supplies |
|------------|-------------------|----------------|--------------------|
| 50%        | 3.90V             | 4.15V          | 1                  |
| 0%         | 0.00V             | 0.50V          | 1                  |

Note: The current share bus will not oscillate during application of AC, or during hot-plug.

### 3.9 Power Management Bus (PMBus\*)

### 3.9.1 Resolution and Range

The resolution for all of the linear formatted commands is very wide. The following table puts boundaries on the expected data. When writing, command errors will be reported for data outside these parameter ranges.

Table 32. Ranges

| Command           | Range of n   | Real Range                   | Format     |
|-------------------|--------------|------------------------------|------------|
| READ_VIN          |              |                              |            |
| MFR_VIN_MIN       | -1 ≤ n ≤ -5  | 0 ≤ x ≤ 511 V                | Linear-11  |
| MFR_VIN_MAX       |              |                              |            |
| READ_IIN          |              |                              |            |
| IIN_OC_WARN_LIMIT | -4 ≤ n ≤ -9  | $0 \le x \le 63 \text{ A}$   | Linear-11  |
| MFR_IIN_MAX       |              |                              |            |
| READ_VOUT         |              |                              |            |
| MFR_VOUT_MIN      | -9           | 0 ≤ x ≤ 127 V                | Linear-16  |
| MFR_VOUT_MAX      |              |                              |            |
| READ_IOUT         | -3 ≤ n ≤ -7  | 0 ≤ x ≤ 127 A                | Linear-11  |
| MFR_IOUT_MAX      | -3 2 11 2 -7 | 0 S X S 127 A                | Lillear-11 |
| READ_TEMP_n       |              |                              |            |
| MFR_TAMBIENT_MIN  | 0 ≤ n ≤ -2   | 0 ≤ x ≤ 1023 C               | Linear-11  |
| MFR_TAMBIENT_MAX  |              |                              |            |
| READ_FAN_SPEED_n  | 5 ≤ n ≤ 0    | 0 ≤ x ≤ 32736 RPM            | Linear-11  |
| READ_POUT         | 0 ≤ n ≤ -5   | 0 ≤ x ≤ 1023 W               | Linear-11  |
| MFR_POUT_MAX      | 0 2 11 2 -0  | 0 S X S 1023 VV              | Lilleal-11 |
| READ_PIN,         |              |                              |            |
| PIN_OC_WARN_LIMIT | 0 ≤ n ≤ -5   | $0 \le x \le 1023 \text{ W}$ | Linear-11  |
| MFR_PIN_MAX       |              |                              |            |
| FAN_COMMAND_n     | 0 ≤ n ≤ -2   | 0 ≤ x ≤ 100 %                | Linear-11  |

**Table 33. PMBus\* Required Accuracy** 

| Output Loading   | 10% - 20%            | > 20% - 50%                   | > 50% - 100%   |  |  |
|------------------|----------------------|-------------------------------|----------------|--|--|
| READ_PIN         | +/-5% at 200W to 100 | % load; +/-10W from idle (30W | ) load to 200W |  |  |
| READ_FAN         | TBD                  |                               |                |  |  |
| READ_IOUT        | +/-5% +/-2% +/-2     |                               |                |  |  |
| READ_TEMPERATURE | +/- 3°C              |                               |                |  |  |

### 3.9.2 PMBus\* Device Addressing

The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined below uses 7 bits (8 bits with LSB zero).

Table 34. PMBus\* Device Addressing

| Address A1/A0  | 0/0       | 0/1       | 1/0       | 1/1       |
|----------------|-----------|-----------|-----------|-----------|
| PMBus* Address | 58h (B0h) | 59h (B2h) | 5Ah (B4h) | 5Bh (B6h) |

### 3.9.3 IPMI FRU Device Addressing

The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined below uses 7 bits (8 bits with LSB zero).

Table 35. IPMI FRU Device Addressing

| Address A1/A0    | 0/0       | 0/1       | 1/0       | 1/1       |
|------------------|-----------|-----------|-----------|-----------|
| IPMI FRU Address | 50h (A0h) | 51h (A2h) | 52h (A4h) | 53h (A6h) |

# 4. Thermal and Acoustic Management

The Intel Server System R2000IP is designed to operate at external ambient temperatures in compliance with ASHARE class A2. Working with integrated platform management, features within the system are designed to move air in a front to back direction, through the system and over critical components in order to prevent overheating and allow the system to operate with best performance.

#### 4.1 Thermal Operation and Configuration Requirements

To keep the system operating within supported maximum thermal limits, the system must meet the following operating and configuration guidelines:

- The system operating ambient is designed for sustained operation up to 35°C (ASHRAE Class A2) with short term excursion based operation up to 45°C (ASHRAE Class A4).
  - The system can operate up to 40°C (ASHRAE Class A3) for up to 900 hours per year
  - The system can operate up to 45°C (ASHRAE Class A4) for up to 90 hours per year
  - System performance may be impacted when operating within the extended operating temperature range
  - There is no long term system reliability impact when operating at the extended temperature range within the approved limits.
- Specific configuration requirements and limitations are documented in the configuration matrix found in the Intel® Server System R2000IP product family Power Budget and Thermal Configuration Guidelines Tool, available as a download online at Intel.com.
- The CPU-1 processor + CPU heat sink must be installed first. The CPU-2 heat sink must be installed at all times, with or without a processor installed.
- Memory Slot population requirements –

NOTE: Specified memory slots can be populated with a DIMM or supplied DIMM Blank. Memory population rules apply when installing DIMMs.

- DIMM Population Rules on CPU-1 Install DIMMs in order; Channels A, B, C, and D¹. Start with1st DIMM (Blue Slot) on each channel, then slot 2. Only remove factory installed DIMM blanks when populating the slot with memory.
- DIMM Population on CPU-2 Install DIMMs in order; Channels E, F, G, and H<sup>1</sup>.
   Start with1st DIMM (Blue Slot) on each channel, then slot 2. Only remove factory installed DIMM blanks when populating the slot with memory.
- The following system configurations require that specific memory slots be populated at all times using either a DIMM or supplied DIMM Blank
- ❖ System Configuration 24x 2.5" hard drive bay or 12x 3.5" hard drive bay configuration + Intel<sup>®</sup> Server Board S2600IP (16 DIMM server board)
  - Memory slot 2 populated on all memory channels
- All hard drive bays must be populated. Hard drive carriers can be populated with a hard drive or supplied drive blank.
- With the system operating, the air duct must be installed at all times
- In single power supply configurations, the 2<sup>nd</sup> power supply bay must have the supplied filler blank installed at all times.
- The system must be configured with dual power supplies for the system to support fan redundancy.
- Thermally, the system can support the following PCI add-in cards.

- Add-in cards with a minimum 100 LFM (0.5 m/s) air flow requirement can be installed in any available add-in card slot
- Add-in cards with a minimum 200 LFM (1 m/s) air flow requirement can be installed in any available add-in card slot.
- Add-in cards with a >200 LFM air flow requirement cannot be supported.
- Note: Most PCI add-in cards have minimum air flow requirements of 100 LFM (0.5m/s). Some high power add-in cards have minimum air flow requirements of 200 LFM (1 m/s). System integrators should verify PCI add-in card air flow requirements from vendor specifications when integrating add-in cards into the system.
- The system top-cover must be installed at all times when the system is in operation. The only exception to this requirement is to hot replace a failed system fan, in which case the top cover can be removed for no more than 3 minutes at a time
- Supported ambient temperature vs processor TDP is as follow:

|   |   | 0      |       |      | ı       |       |        | (8)    |        |               |         |
|---|---|--------|-------|------|---------|-------|--------|--------|--------|---------------|---------|
| Notes:  |   |        |       |      |         |       |        |        |        |               |         |
| 1. For A3/A4 individual PS sel                            | ection:   |        |       |      |         |       |        |        |        |               |         |
| 1) For dual power supply co                               | onfiguration, power budget must fit within single power supply rated load and |        |       |      |         |       |        |        |        |               |         |
| be installed in dual configurat                           |   |        |       |      |         |       |        |        |        |               |         |
|   | configuration, power budget must be sized with 30% margin to single power     |        |       |      |         |       |        |        |        |               |         |
| supply rated load.  | Adapter card specifications typically include environmental requirements      |        |       |      |         |       |        |        |        |               |         |
|   | ating ambient and minimum airflow. These PCI slots are limited to cards that  |        |       |      |         |       |        |        |        |               |         |
| require 100LFM or less.                                   |   |        |       |      |         |       |        |        |        |               |         |
|   | 35W-8C may have some performance impact.                                      |        |       |      |         |       |        |        |        |               |         |
|   | ome performance impact during fan failures or ambient excursions.             |        |       |      |         |       |        |        |        |               |         |
| GPGPU cards may have per     LV refers to low voltage DIN | formance impact during ambient excursions                                     | Bas    | e Su  | stem | Ras     | e Su  | stem   |        |        |               |         |
|   | n the table, only Rank and Width are required. Capacity is not required.      |        | SKU   |      | 1000000 | SKU   |        | Base : | System |               |         |
|   | only be installed with 95W processor and DRx8 or equivalent memory            | 100000 | 2312  |      |         | 230   |        |        | Us:    |               |         |
| 9. "Fan Fail Support" indicate                            | s if fan fail can be supported with specified configuration in each column.   | R      | 2224  | HP   | F       | 221   | 6IP    | R22    | 08IP   |               |         |
| ASHRAE  | Classifications   | _      | -     | A4   | 1000    | АЗ    | 35,455 | A2     | А3     |               |         |
|   | Max Ambient   | _      | 40C   | 45C  | 35C     | 400   | 45C    | 35C    | 40C    |               |         |
| Cooling (See note 9)                                      | Redundant Fan Configuration   | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| 200,000   | Fan Fail Support  | •      | 1000  |      | •       |       |        | •      | 100    |               |         |
| PS (See note 1)   | Power Supplies  |        | ee To | ol   |         | ee To | ool    | 22     | Tool   | < See note 1  |         |
|   | EP, 60w, 6C (Intel® Xeon® processor E5-2630L)                                 | •      | 72    |      | •       | •     |        | •      | •      | < see note 4  |         |
| ( <del>4</del> )  | EP, 70w, 8C (Intel® Xeon® processor E5-2650L)                                 | •      | •     |      | •       | •     | •      | •      | •      | < see note 4  |         |
| and   | EP, 95w, 6C (Intel® Xeon®processor E5-2620 , E5-2630, E5-2640)                | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| Processors ( See Notes 3                                  | EP, 95w, 8C (Intel® Xeon®processor E5-2650, E5-2660)                          |        | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| N   | EP, 115w, 8C (Intel® Xeon®processor E5-2665, E5-2670)                         | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| Se  | EP, 130w, 6C (Intel® Xeon® processor E5-2667)                                 | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| ors (   | EP, 130w, 8C (Intel® Xeon® processor E5-2680)                                 | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| Sessi   | EP, 135w, 8C (Intel® Xeon® processor E5-2690)                                 | •      |       | -    | •       |       | 0.255  | •      | 4      | < See notes 3 | and 4   |
| Proc  | EP, 80w, 2C (Intel® Xeon® processor E5-2637)                                  | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  |         |
| <b>a</b>  | EP, 80w, 4C (Intel® Xeon® processor E5-2603, E5-2609)                         | •      | •     | •    | •       | •     | •      | •      | •      | < see note 4  | 10.5475 |
|   | EP, 130w, 4C (Intel® Xeon® processor E5-2643)                                 | •      |       |      | •       |       |        | •      |        | < See notes 3 | and 4   |
| e P   | Dual Rank x8  | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| Type<br>6 and   | Dual Rank x4  | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| Memory Type<br>(See note 6 and<br>7)                      | Quad Rank x8  | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| Se I  | Quad Rank x4  | •      | 25    |      | •       |       |        | •      | •      |               |         |
|   | Load Reduced DIMM   | •      | 0     | 0    | •       |       |        | •      | 14     |               |         |
| Add-in Cards (See note 2)                                 | PCI Cards   | •      | 0     | 0    | •       | •     | •      | •      | •      | < See note 2  |         |
|   | Intel® Integrated RAID Modules (Mezzanine cards)                              | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| <u>(C)</u>  | AXX10GBTWLIOM - Dual 10GBASE-T IO Module                                      | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| <u> </u>  | AXX10GBNIAIOM - Dual SFP+ port 10GbE IO Module                                | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| Module (3)  | AXX1FDRIBIOM - Single Port FDR Infiniband IO Module                           | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| 2   | AXX2FDRIBIOM - Dual Port FDR Infiniband IO Module                             | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
|   | AXX4P1GBPWLIOM - Quad Port 1GbE IO Module                                     | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
| 300011444641157000 30 0044                                | Active up to 300W   | ــــــ |       |      |         |       |        |        |        | < See note 5  |         |
| GPGPU (See note 5)  | Active up to 225W   |        |       |      |         |       |        |        |        | < See note 5  |         |
|   | Passive up to 75W   |        |       |      |         |       |        |        |        |               |         |
|   | BBU (rated to 45C)  | •      | 3     | 9    | •       |       |        | •      |        |               |         |
| Battery Backup (See note 8)                               | Supercap (rated to 55C)   | •      | •     | •    | •       | •     | •      | •      | •      |               |         |
|   | Cache Offload Module (rated to 55C)   | •      |       | •    | •       | •     | •      | •      | •      |               |         |

### 4.2 Thermal Management Overview

In order to maintain comprehensive thermal protection and meanwhile deliver best system acoustic as well as fan power efficiency, an intelligent Fan Speed Control (FSC) and thermal

management technology (mechanism) is developed. Options reserved for end users to adjust parameter settings based on the actual system configuration and usage in BIOS interface with path: BIOS > Advanced > System Acoustic and Performance Configuration. Refer to below to setup the system thermally right.

### 4.2.1 Set Throttling Mode

Select the most appropriate memory thermal throttling mechanism for memory sub-system from [Auto], [DCLTT], [SCLTT] and [SOLTT].

- [Auto] BIOS automatically detect and identify the appropriate thermal throttling mechanism based on DIMM type, airflow input, and DIMM sensor availability.
- [DCLTT] Dynamic Closed Loop Thermal Throttling: for the SOD DIMM with system airflow input
- [SCLTT] Static Close Loop Thermal Throttling: for the SOD DIMM without system airflow input
- [SOLTT] Static Open Loop Thermal Throttling: for the DIMMs without sensor on DIMM (SOD)

The default setting is [Auto].

#### 4.2.2 Altitude

Select the proper altitude that the system is distributed from [300m or less], [301m-900m], [901m-1500m], [Above 1500m] options. Lower altitude selection can lead to potential thermal risk. And higher altitude selection provides better cooling but with undesired acoustic and fan power consumption. If the altitude is known, higher altitude is recommended in order to provide sufficient cooling. The default setting is [301m – 900m].

#### 4.2.3 Set Fan Profile

[Performance] and [Acoustic] fan profiles are available to select. The Acoustic mode offers best acoustic experience and appropriate cooling capability covering mainstream and majority of the add-in cards. Performance mode is designed to provide sufficient cooling capability covering all kinds of add-in cards on the market. The default setting is [Performance]

#### 4.2.4 Fan PWM Offset

This feature is reserved for manual adjustment to the minimum fan speed curves. The valid range is from [0 to 100] which stands for 0% to 100% PWM adding to the minimum fan speed. This feature is valid when Quiet Fan Idle Mode is at Enabled state. The default setting is [0].

#### 4.2.5 Quiet Fan Idle Mode

This feature can be [Enabled] or [Disabled]. If enabled, the fan will either stopped or shift to a lower speed when the aggregate sensor temperatures are satisfied indicating the system is at ideal thermal/light loading conditions. When the aggregate sensor temperatures not satisfied, the fan will shift back to normal control curves. If disabled, the fan will never stopped or shift into lower fan speed whatever the aggregate sensor temperatures are satisfied or not. The default setting is [Disabled]

**Note**: The above features may or may not be in effective depends on the actual thermal characters of a specific system. Refer to specific system for additional information.

#### 4.2.6 Fan and HDD Configuration

The Intel® Server System R2000IR consists six 60x38mm system fans providing cooling for all ingredients inside the enclosure.

All the fans are Pulse Width Modulated (PWM) 4 wire/pin fans. The fan headers are connected to motherboard with below sequence. Misconnect will potentially lead to thermal risk or undesired acoustic.

- SYS FAN 1 Header #1 connect to one 60x38mm system fan
- SYS FAN 2 Header #1 connect to one 60x38mm system fan
- SYS FAN 3 Header #1 connect to one 60x38mm system fan
- SYS FAN 4 Header #1 connect to one 60x38mm system fan
- SYS FAN 5 Header #1 connect to one 60x38mm system fan
- SYS FAN 6 Header #1 connect to one 60x38mm system fan
- CPU 1 FAN connect reserved
- CPU 2 FAN connect reserved
- REAR FAN reserved

The Intel® Server System R2000IR supports up to 12x3.5" HDDs and 24x2.5" HDDs.

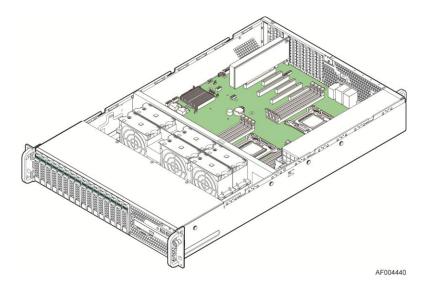


Figure 22. System Overview for Thermal Management

**Note**: If Quiet Fan Idle Mode is enabled, with combination of Altitude set to [300m or less] or [301m-900m] and Fan Profile set to [Acoustic] mode, the core fan will stop running when the aggregate sensor temperatures are satisfied indicating the system is at good thermal/light loading conditions. For other scenarios, the core fan will maintain a minimum RPM.

#### 4.2.7 Acoustic

The Intel® Server System R2000IR acoustic is measured with typical configuration and typical operating working conditions.

| System Configuration | System SKU 1,2 |
|----------------------|----------------|
| CPU                  | 135W (2x)      |
| Memory               | DRx8 (16x)     |

| Disk/Optical      | SATA 3.5" (6x)          |
|-------------------|-------------------------|
| Gfx/add-in card   | PCI-e card (3x)         |
| Others            | Roc Mezz card           |
| PSU               | 750W (2x)               |
| Declared Acoustic | Idle: 5.7BA             |
|                   | TO1: 6.1BA <sup>3</sup> |
|                   | TO2: 6.2BA <sup>4</sup> |

#### Notes:

- System is at or below 900m altitude and set to acoustic mode.
   Quiet Fan Idle Mode is enabled.

- TO1 Typical operating mode 1: processor and HDD stressed.
   TO2 Typical operating mode 2: processor, memory, HDD stressed.

#### 4.3 Processor Heatsink

A heatsink is included in the system package. This heatsink is designed for optimal cooling and performance. To achieve better cooling performance, you must properly attach the heatsink bottom base with TIM (thermal interface material), the heatsink is required if necessary.

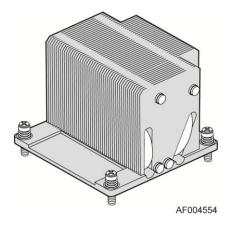


Figure 23. Processor Heatsink Overview

### 4.4 System cooling Fans

Six 80x38-mm fans provide the primary airflow for the system. The system is designed for fan redundancy. Should a single fan fail, the remaining four system fans along with platform management will provide the necessary air flow and other platform adjustments to maintain system thermals. Fan redundancy is lost if more than one fan is in a failed state.

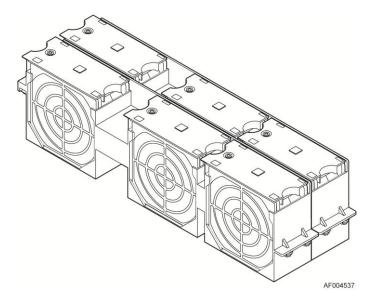


Figure 24. System Fan Assembly

The system fan assembly is designed for ease of use and supports several features.

- Each fan is hot-swappable.
- Each fan is designed for tool-less insertion and extraction from the fan assembly.
- Fan speed for each fan is controlled by integrated platform management as controlled by the integrated BMC on the server board. As system thermals fluctuate high and low, the

integrated BMC firmware will increase and decrease the speeds to specific fans within the fan assembly to regulate system thermals.

- Each fan has a tachometer signal that allows the Integrated BMC to monitor their status.
- On top of each fan is an integrated fault LED. Platform management illuminates the fault LED for the failing fan.
- Each fan has 6-pin wire harness that connects to a matching connector on the server board.

| Pin | Signal Name |
|-----|-------------|
| 1   | GND         |
| 2   | 12V         |
| 3   | TACH IN     |
| 4   | PWM OUT     |
| 5   | PRESENT     |
| 6   | FAULT       |

**Table 36. System Fan Connector Pin-out** 

### 4.5 Power Supply Fan

Each installed power supply module includes one 40-mm fan. It is responsible for airflow through the power supply module. This fan is NOT managed by platform management. Should this fan fail, the power supply will continue to operate until its internal temperature reaches an upper critical limit. The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an over-temperature protection condition, the power supply module will shut down.

### 4.6 Air Duct Module

The chassis requires the use of an air duct module to direct airflow over critical areas within the system. The following provides a summary and description of Air Duct Module.

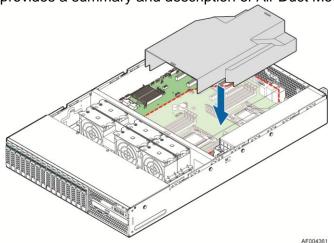


Figure 25. Air Duct Module

# 5. System Storage and Peripheral Drive Bays

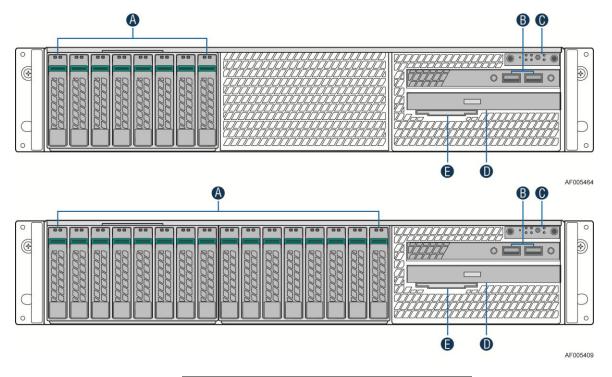
The Intel® Server System R2000IP4 product family has support for many storage device options, including:

- Hot Swap 2.5" Hard Disk Drives
- Hot Swap 3.5" Hard Disk Drives
- SATA Optical Drive
- SATA Solid State Devices (SSDs)
- Low Profile (2mm) eUSB Solid State Device (eUSB SSD)

Support for different storage and peripheral device options will vary depending on the system SKU. This section will provide an overview of each available option.

### 5.1 2.5" Hard Disk Drive Support

The server is available in 2.5" hard disk configurations of 8, 16, and 24 drives as illustrated below.



| Label | Description                  |
|-------|------------------------------|
| Α     | 2.5" Hard Drive Bays         |
| В     | USB Ports                    |
| С     | Front Control Panel          |
| D     | SATA Optical Drive(Optional) |
| E     | System Label Pull-out        |

Figure 26. 2.5" Hard Drive Bay - 8 and 16 Drive Configuration

Figure 27. 2.5" Hard Drive Bay - 24 Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 2.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

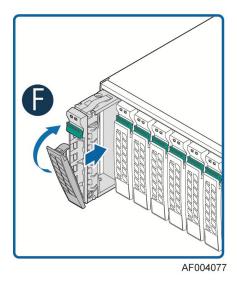
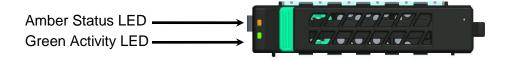


Figure 28. 2.5" Hard driver installation

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.



**Table 37. Drive Status LED States** 

|       | No access and no fault                       |  |  |  |  |
|-------|--|--|--|--|--|
| Amber | Mmber Solid On Hard Drive Fault has occurred |  |  |  |  |
|       | Blink  | RAID rebuild in progress (1 Hz), Identify (2 Hz) |  |  |  |

Condition **Drive Type Behavior** SAS LED stays on Power on with no drive activity SATA LED stays off SAS LED blinks off when processing a command Power on with drive activity Green SATA LED blinks on when processing a command SAS LED stays off Power on and drive spun down SATA LED stays off SAS LED blinks Power on and drive spinning up SATA LED stays off

**Table 38. Drive Activity LED States** 

### 5.1.1 2.5" Drive Hot-Swap Backplane Overview

Depending on the number of hard disk drives supported by a given system SKU, a system can be configured with 1, 2, or 3 eight drive backplanes. Each backplane is attached to the back of the drive bay assembly.

On the front side of each backplane are mounted eight hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.

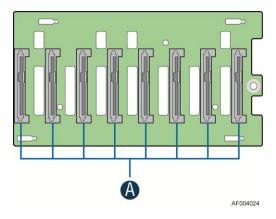
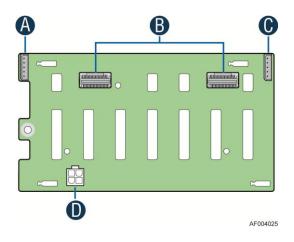


Figure 29. 2.5" Hard Drive Backplane front side

On the backside of each backplane are several connectors. The following illustration identifies each.



| Label | Description   |
|-------|---|
| Α     | SMBus*-out cable connector – From Server board or other backplane |
| В     | 4-port Mini-SAS cable connectors                                  |
| С     | SMBus*-in cable connector for multi-backplane support             |
| D     | Power connector   |

Figure 30. 2.5" Hard Drive Backplane backside

**A** – Multi-port Mini-SAS Cable Connectors – The backplane includes two multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards.

**B and D** – SMBus\* Cable Connectors – The backplane includes two 1x5 cable connectors used as a management interface between the server board and the installed backplanes. In systems configured with multiple backplanes, a short jumper cable is attached between backplanes, with connector B used on the first board and connector D used on the second board, extending the SMBus\* to each installed backplane.

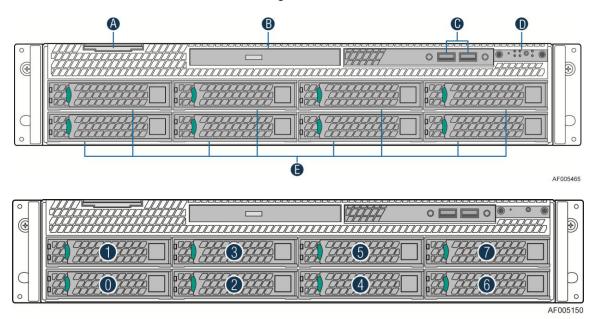
**C** – Power Harness Connector – The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to each installed backplane from a multi-connector power cable harness from the server board.

#### 5.1.2 Cypress\* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress\* CY8C22545 Programmable System-on-Chip (PSoC\*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

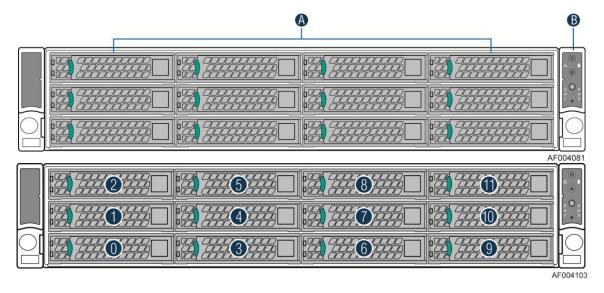
### 5.2 3.5" Hard Disk Drive Support

The server is available in 3.5" hard disk configurations of 8 and 12 drives as illustrated below.



| Label | Description           |
|-------|-----------------------|
| Α     | System label pull-out |
| В     | SATA Optical Drive    |
| С     | USB Ports             |
| D     | Front Control Panel   |
| E     | 3.5" Hard Drive Bays  |

Figure 31. 3.5" Hard Drive Bay - 8 Drive Configuration



| Label | Description          |
|-------|----------------------|
| А     | 3.5" Hard Drive Bays |
| В     | Front Control Panel  |

Figure 32. 3.5" Hard Drive Bay - 12 Drive Configuration

The drive bay can support either SATA or SAS hard disk drives. Mixing of drive types within the hard drive bay is not supported. Hard disk drive type is dependent on the type of host bus controller used, SATA only or SAS. Each 3.5" hard disk drive is mounted to a drive tray, allowing for hot swap extraction and insertion. Drive trays have a latching mechanism that is used to extract and insert drives from the chassis, and lock the tray in place.

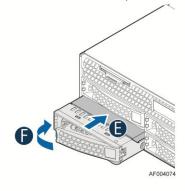
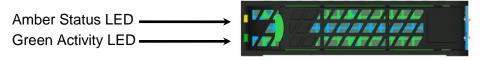


Figure 33. 3.5" Hard driver installation

Light pipes integrated into the drive tray assembly direct light emitted from Amber drive status and Green activity LEDs located next to each drive connector on the backplane, to the drive tray faceplate, making them visible from the front of the system.



**Table 39. Drive Status LED States** 

|       | Off      | No access and no fault                           |  |  |
|-------|----------|--|--|--|
| Amber | Solid On | Hard Drive Fault has occured                     |  |  |
|       | Blink    | RAID rebuild in progress (1 Hz), Identify (2 Hz) |  |  |

**Table 40. Drive Activity LED States** 

|       | Condition                       | Drive Type | Behavior                                 |
|-------|---------------------------------|------------|--|
| Green | Power on with no drive activity | SAS        | LED stays on                             |
|       | Power on with no drive activity | SATA       | LED stays off                            |
|       | Dower on with drive estivity    | SAS        | LED blinks off when processing a command |
|       | Power on with drive activity    | SATA       | LED blinks on when processing a command  |
|       | Power on and drive spun down    | SAS        | LED stays off                            |
|       |                                 | SATA       | LED stays off                            |
|       | Dower on and drive eninning up  | SAS        | LED blinks                               |
|       | Power on and drive spinning up  | SATA       | LED stays off                            |

#### 5.2.1 3.5" Drive Hot-Swap Backplane Overview

Systems with 8 or 12 drive configurations have their own unique backplane. Both 8 and 12 drive backplanes share identical features. The following will be used to describe the features of both backplanes. Differences between the two will be noted.

The backplanes mount to the back of the drive bay assembly. On the front side of each back plane are mounted eight or twelve hard disk drive interface connectors (A), each providing both power and I/O signals to attached hard disk drives.

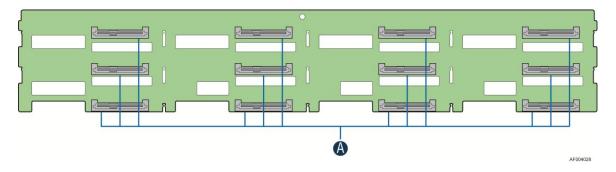


Figure 34. 3.5" Drive Hot-Swap Backplane Overview

Behind each backplane are several connectors. The following illustration identifies these connectors.

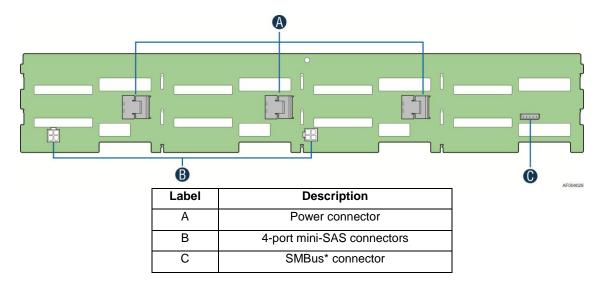


Figure 35. 3.5" Hard Drive Backplane backside

**A –** Power Harness Connector - The backplane includes a 2x2 connector supplying power to the backplane. Power is routed to the backplane from a power cable harness from the server board

**B –** 4-port Mini-SAS Connectors – The backplane includes two or three multi-port mini-SAS cable connectors, each providing I/O signals for four SAS/SATA hard drives on the backplane. Cables can be routed from matching connectors on the server board, add-in SAS/SATA RAID cards, or optionally installed SAS expander cards. Each mini-SAS connector will include a silk-screen identifying which drives the connector supports; Drives 0-3, Drives 4-7, and Drives 8-11.

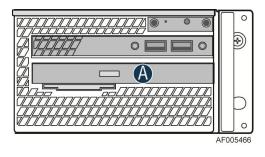
**C –** SMBus\* Cable Connectors – The backplane includes a 1x5 cable connector used as a management interface to the server board.

### 5.2.2 Cypress\* CY8C22545 Enclosure Management Controller

The backplanes support enclosure management using a Cypress\* CY8C22545 Programmable System-on-Chip (PSoC\*) device. The CY8C22545 drives the hard drive activity/fault LED, hard drive present signal, and controls hard drive power-up during system power-on.

### 5.3 Optical Drive Support (optional)

Systems configured with eight 3.5" hard drive bays or up to sixteen 2.5" hard drive bays also include support for an optical drive bay 'A' as illustrated below.



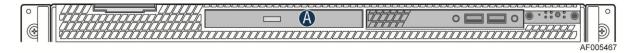


Figure 36. Opitcal driver support

### 5.4 eUSB SSD Suport

The system provides support for a eUSB SSD storage device. A 2x5-pin connector labeled "eUSB SSD" near the rear I/O section of the server board is used to plug this small flash storage device into.

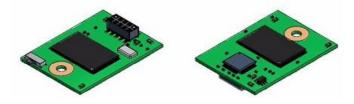


Figure 37. eUSB SSD Suport

- 2 wire small form factor Universal Serial Bus 2.0 (Hi-Speed USB) interface to host.
- Read Speed up to 35 MB/s and write Speed up to 24 MB/s.
- Capacity range from 256GB to 32GB.
- Support USB Mass Storage Class requirements for Boot capability.

### 5.5 SAS Expander Support Options

The system is designed to support SAS Expander cards for storage configurations that require more than eight hard disk drives.

The following table outlines the different Intel SAS Expander options available and which one to use for given hard disk drive configurations.

Table 41. SAS Expander Support Options

Installation type Hard Drive

| Intel <sup>®</sup> SAS Expander                              | Installation type | Hard Drive Configuration                |
|--|-------------------|---|
| 24 Port PCIe Intel <sup>®</sup> RAID Expander Card RES2SV240 | PCIe add-in card  | 3.5" Hard Disk drive bay configurations |
| 24 Port Internal Intel® RAID Expander                        | Internal mount    | 2.5" Hard Disk drive bay configurations |
| 36 Port Internal Intel® RAID Expander                        | Internal mount    | 2.5" Hard Disk drive bay configurations |

### 5.5.1 24-Port PCIe Intel<sup>®</sup> RAID Expander Card RES2SV240

For large storage configurations that utilize a drive bay supporting twelve 3.5" hard disk drives, a 24-Port PCIe Intel<sup>®</sup> RAID Expander Card RES2SV240 may be installed into any available PCIe add-in slot. Technical Specifications are as follows:

Intel Order Code RES2SV240 (includes 6 cables) RES2SV240NC (no cables) LSI\* LSISAS2x24 24-Port Serial Attached SCSI/SATA Expander chip **Embedded Processor** Intel® RAID Controllers (SAS-2) Compatibility Intel® Integrated RAID Modules (SAS-2) RAID or non-RAID mode 24 total sub-divided into 6 guad port by 8087 (Mini-SAS) connectors SAS/SATA Ports 8 MB in an updateable flash ROM Firmware **Enclosure Management SGPIO Operating Temperature** Maximum ambient: 50°C (45°C with optional BBU) Operating Voltage Cables Included Six with 8087 (Mini-SAS) to 8087 (Mini-SAS) connectors (2 short and 4 long)

Table 42. Intel® RAID Expander Card RES2SV240 Series Basic Feature

For additional information on the Intel<sup>®</sup> RAID Expander Card RES2SV240, please reference the *Intel*<sup>®</sup> *RAID Expander Card RES2SV240 Hardware Users Guide*, Intel Document Order # E93121-003.

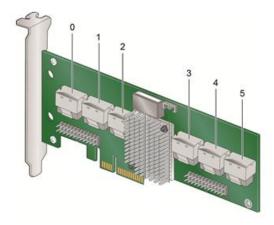


Figure 38. 24 Port PCIe Intel® RAID Expander Card RES2SV240

Each connector on the SAS expander card can be used as a "cable in" (SAS Controller to SAS Expander) or "cable out" (SAS Expander to Hot Swap Backplane) type connector. However, for contiguous drive mapping (0-12), cable routing differs when using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller vs. using the embedded SCU ports.

#### 5.5.1.1 Cable Routing using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller

To ensure contiguous drive mapping when using a x8 wide-port capable 6 Gb SAS/SAS RAID controller, the system must be cabled as follows:

- Cables from the SAS Expander to the hot swap backplane must be connected in order: 0 – 2.
- The cables from the SAS controller can be attached to any of the remaining connectors on the SAS expander card.

#### 5.5.1.2 Cable Routing using the embedded SCU ports

**Note**: The following may also be applied when using any 3 Gb SAS/SAS RAID Controller.

For storage configurations that utilize up to 12 hard disk drives for storage only and an internally mounted SSD as a boot device, the system must be configured as follows to ensure contiguous drive mapping (0 - 12):

- At least one internally mounted SSD device must be attached to the AHCI controller (SATA\_0 or SATA\_1 on the server board) and used as a boot device.
- Cables from the SAS Expander to the hot swap backplane must be connected in order: **Connector 1 Connector 3**.
- The SCU\_0 or 3G SAS/SAS RAID (0-3) connector is cabled to the first mini-SAS connector on the hot swap backplane
- The SCU\_1 or 3G SAS/SAS RAID (4-7) connector is cable to Connector\_0 on the SAS expander card.

For storage configurations that require utilizing a hard disk drive as the boot device, the system must be cabled as follows to ensure a boot device is found and contiguous drive mapping (0-12).

- The <u>SCU\_0 (0-3</u>) connector on the server board is cabled to the first mini-SAS connector on the hot swap backplane
- The <u>SCU\_1 (4-7)</u> connector on the server board is cable to <u>Connector\_0</u> on the SAS expander card.
- Cables from the SAS Expander to the hot swap backplane must be connected in order: Connector 1- Connector 3.

**Note**: Current SCU controller design limitations prevent any hard drive attached to a SAS expander card from being a boot device when both SCU connectors are attached to the SAS expander card.

Please reference the *Intel® Server System R2000IP Product Family Service Guide* for cable routing diagrams illustrating a variety of different storage configurations.

#### 5.5.2 24-Port and 36-Port Internal Intel RAID Expander Cards

For large storage configurations that utilize more than eight 2.5" hard disk drives, the system may be configured with an internally mounted SAS expander card mounted directly behind the drive bay assembly as shown in the following illustration. SAS expander selection is dependent on the desired SAS controller configuration.

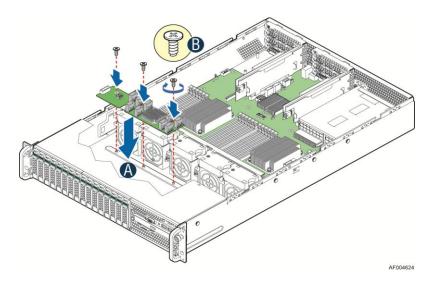


Figure 39. Internal SAS Expander Installation

The following diagrams are used to help identify the mini-SAS connectors found on the SAS expander cards. Care should be taken when connecting connectors from the SAS expander to the connectors on the backplane because each connector is pre-programmed at the factory to provide specific drive identification mapping. Improper connections may provide undesirable drive mappings.

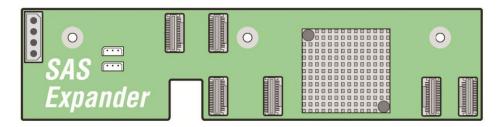


Figure 40. Internal 24-Port SAS Expander Card

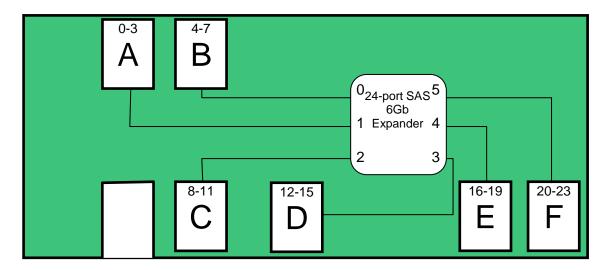


Figure 41. 24-Port Expander SAS Connector/Drive Identification Block Diagram

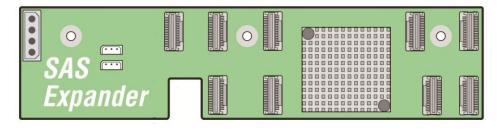


Figure 42. Internal 36-Port SAS Expander Card

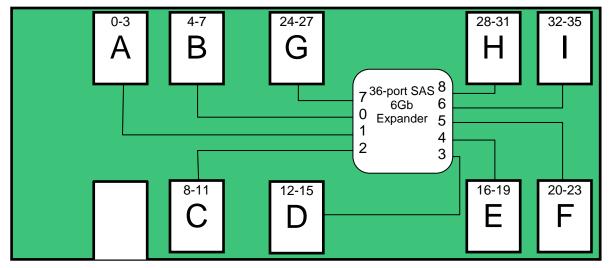


Figure 43. 36-Port Expander SAS Connector/Drive Identification Block Diagram

Each connector on the SAS expander card can be used as a "cable in" (SAS Controller to SAS Expander) or "cable out" (SAS Expander to Hot Swap Backplane) type connector. However, for contiguous drive mapping (0 - 16 or 0 - 24), cable routing differs when using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller vs. using the embedded SCU ports.

#### 5.5.2.1 Cable Routing using a x8 wide-port capable 6 Gb SAS/SAS RAID Controller

To ensure contiguous drive mapping when using x8 wide-port capable 6 Gb SAS/SAS RAID Controller with a SAS expander card, the system must be cabled as follows:

- Cables from the SAS Expander to the hot swap backplane must be connected in order:
   A D for 16-drive configurations, and A F for 24 drive configurations.
- The cables from the SAS controller can be attached to any of the remaining connectors on the SAS expander card.

#### 5.5.2.2 Cable Routing using the embedded SCU ports

**Note**: The following may also be applied when using any 3 Gb SAS/SAS RAID Controller.

For storage configurations that utilize up to 16 or 24 hard disk drives for storage only and an internally mounted SSD as a boot device, the system must be configured as follows to ensure contiguous drive mapping (0 – 16 or 0-24):

 At least one internally mounted SSD device must be attached to the AHCI controller (SATA\_0 or SATA\_1 on the server board) and used as a boot device.

- Cables from the SAS Expander to the hot swap backplane must be connected in order:
   B E for 16-drive configurations, and B G for 24 drive configurations.
- The SCU\_0 or 3G SAS/SAS RAID (0-3) connector is cabled to the first mini-SAS connector on the hot swap backplane
- The SCU\_1 or 3G SAS/SAS RAID (4-7) connector is cable to Connector A on the SAS expander card.

For storage configurations that require utilizing a hard disk drive as the boot device, the system must be cabled as follows to ensure a boot device is found and for contiguous drive mapping (0-16 or 0-24).

- The <u>SCU\_0 (0-3</u>) connector on the server board is cabled to the first mini-SAS connector on the hot swap backplane
- The <u>SCU\_1 (4-7)</u> connector on the server board is cable to <u>Connector\_A</u> on either the 24-port or 36-port SAS expander card.
- Cables from the SAS Expander to the hot swap backplane must be connected in order: B F on the 24-port expander card, and B G on the 36-port expander card.

**Note**: Current SCU controller design limitations prevent any hard drive attached to a SAS expander card from being a boot device when both SCU connectors are attached to the SAS expander card.

Please reference the *Intel® Server System R2000IP Product Family Service Guide* for cable routing diagrams illustrating a variety of different storage configurations.

#### 5.5.3 Protocol Support

Each port on the expander cards support SAS devices, SATA II devices, or both using SSP, SMP, STP, and SATA II as follows:

- Serial SCSI Protocol (SSP) to enable communication with other SAS devices.
- SATA II Protocol to enable communication with other SATA II devices.
- Serial Management Protocol (SMP) to share topology management information with expanders.
- Serial Tunneling Protocol (STP) support for SATA II through expander interfaces.
- SAS protocol, described in the Serial Attached SCSI (SAS) Standard, version 2.0
- SFF-8485 protocol, using the Serial GPIO (SGPIO) interface provided by the expander.

#### 5.5.4 Features

- Supports both Serial Attached SCSI and Serial ATA devices
- 6.0 Gbit/s, 3.0 Gbit/s, and 1.5 Gbit/s data transfer rate
- SFF-8087 mini-SAS connectors
- Output mini-SAS connectors support sideband SGPIO as per SFF-8485 specification
- Provides a low-latency connection to create and maintain transparent access to each connected SAS/SATA physical drive
- Staggered spin-up
- Hot Plug
- Native Command Queuing
- Allows multiple initiators to address a single target (in a fail-over configuration)

### 6. Front Control Panel and I/O Panel Overview

All system configurations will include a Control Panel on the front of the system providing push button system controls and LED indicators for several system features. Systems configured with eight 3.5" hard drive bays or up to sixteen 2.5" hard drive bays will also include an I/O Panel providing additional system I/O features. This section describes the features and functions of both front panel options.

#### 6.1 I/O Panel Features

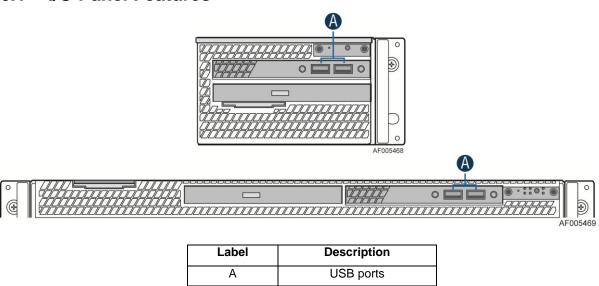


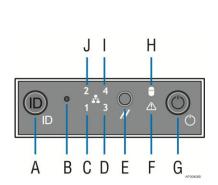
Figure 44. Front I/O Panel Features

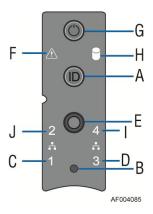
**A – Video connector** – The front I/O Panel video connector gives the option of attaching a monitor to the front of the system. When BIOS detects that a monitor is attached to the front video connector, it disables the video signals routed to the on-board video connector on the back of the system. Video resolutions from the front video connector may be lower than that of the rear on-board video connector. A short video cable should be used for best resolution. The front video connector is cabled to a 2x7 header on the server board labeled "FP Video".

**B – USB Ports** – The front I/O panel includes two USB ports. The USB ports are cabled to a 2x5 connector on the server board labeled "FP USB".

#### 6.2 Control Panel Features

The system includes a control panel that provides push button system controls and LED indicators for several system features. Depending on the hard drive configuration, the front control panel may come in either of two formats; however, both provide the same functionality. This section will provide a description for each front control panel feature.





| Label | Description                                  |   | Description                         |
|-------|--|---|-------------------------------------|
| Α     | System ID Button w/Integrated LED            |   | System Status LED                   |
| В     | NMI Button (recessed, tool required for use) | G | Power/Sleep Button w/Integrated LED |
| С     | NIC-1 Activity LED                           | Н | Hard Drive Activity LED             |
| D     | NIC-3 Activity LED                           | I | NIC-4 Activity LED                  |
| Е     | System Cold Reset Button                     | J | NIC-2 Activity LED                  |

Figure 45. Front Control Panel Features

**A – System ID Button w/Integrated LED** – Toggles the integrated ID LED and the Blue server board ID LED on and off. The System ID LED is used to identify the system for maintenance when installed in a rack of similar server systems. The System ID LED can also be toggled on and off remotely using the IPMI "Chassis Identify" command which will cause the LED to blink for 15 seconds.

**B – NMI Button** – When the NMI button is pressed, it puts the server in a halt state and issues a non-maskable interrupt (NMI). This can be useful when performing diagnostics for a given issue where a memory download is necessary to help determine the cause of the problem. To prevent an inadvertent system halt, the actual NMI button is located behind the Front Control Panel faceplate where it is only accessible with the use of a small tipped tool like a pin or paper clip.

**C, D, I and J – Network Activity LEDs** – The Front Control Panel includes an activity LED indicator for each on-board Network Interface Controller (NIC). When a network link is detected, the LED will turn on solid. The LED will blink once network activity occurs at a rate that is consistent with the amount of network activity that is occurring.

**E – System Cold Reset Button** – When pressed, this button will reboot and re-initialize the system.

**F – System Status LED** – The System Status LED is a bi-color (Green/Amber) indicator that shows the current health of the server system. The system provides two locations for this feature; one is located on the Front Control Panel, the other is located on the back edge of the server board, viewable from the back of the system. Both LEDs are tied together and will show the same state. The System Status LED states are driven by the on-board platform management sub-system. The following table provides a description of each supported LED state.

**G – Power/Sleep Button** – Toggles the system power on and off. This button also functions as a sleep button if enabled by an ACPI compliant operating system. Pressing this button will send a signal to the integrated BMC, which will either power on or power off the system. The integrated LED is a single color (Green) and is capable of supporting different indicator states as defined in the following table.

Table 43. Power/Sleep LED Functional States

| State     | Power Mode | LED                           | Description  |
|-----------|------------|-------------------------------|--|
| Power-off | Non-ACPI   | Off                           | System power is off, and the BIOS has not initialized the chipset.                                     |
| Power-on  | Non-ACPI   | On                            | System power is on but Bios has not initialized the chipset yet  |
| S5        | ACPI       | Off                           | Mechanical is off, and the operating system has not saved any context to the hard disk.                |
| S1        | ACPI       | ~1 Hz blink at 50% duty cycle | DC power is still on. The operating system has saved context and gone into a level of low-power state. |
| S0        | ACPI       | on                            | System and the operating system are up and running.  |

**H – Drive Activity LED** – The drive activity LED on the front panel indicates drive activity from the on-board hard disk controllers. The server board also provides a header giving access to this LED for add-in controllers.

# Appendix A: Integration and Usage Tips

This section provides a list of useful information that is unique to the Intel<sup>®</sup> Server System R2000IP Product Family and should be kept in mind while configuring your server system.

- Only the Intel<sup>®</sup> Xeon<sup>®</sup> processor E5-2600 product family is supported in this Intel server system. Previous generation Intel<sup>®</sup> Xeon<sup>®</sup> processors are not supported.
- For best system performance, follow memory population guidelines as specified in the Intel® Server Board S2600IP Technical Product Specification.
- For best system performance, follow all thermal configuration guidelines as specified in this document.
- The CPU-1 processor + CPU heat sink must be installed first. The CPU-2 heat sink must be installed at all times, with or without a processor installed
- DIMM slots E1 thru H2 are only supported when CPU-2 is installed.
- PCIe slot (4-7) is only functional when two CPUs are installed.
- The Mini-SAS connector labeled "SCU\_1 (4-7)" on the server board is only functional when an appropriate Intel® RAID C600 Upgrade Key is installed.
- Many integrated on-board SAS and RAID options are available by installing any of several available Intel<sup>®</sup> RAID C600 Upgrade Keys.
- The FRUSDR utility must be run after the hardware integration is complete in order to load the proper Sensor Data Records for the server chassis onto the server board.
- Make sure the latest system software is loaded on the server. This includes System BIOS, BMC Firmware, ME Firmware and FRUSDR. The latest system software can be downloaded from the Intel web site.

# Glossary

| ACA Australian Communication Authority ANSI American National Standards Institute BMC Baseboard Management Controller BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit If C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe' Peripheral Component Interconnect Express' PCI-X Peripheral Component Interconnect Express' | Word/Acronym     | Definition                                  |  |
|--|------------------|---|--|
| BMC Baseboard Management Controller BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I*C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Extended PFC Power Factor Correction PFC Power Factor Correction POST Power- on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single-Ended THD Total Harmonic Distortion USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | ACA              | Australian Communication Authority          |  |
| BIOS Basic Input/Output System CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | ANSI             | American National Standards Institute       |  |
| CMOS Complementary Metal-oxide-semiconductor D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power- Or Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | BMC              | Baseboard Management Controller             |  |
| D2D DC-to-DC EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I*C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single-Ended THD Total Harmonic Distortion USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | BIOS             | Basic Input/Output System                   |  |
| EMP Emergency Management Port FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time Between Failure MTTR Mean Time Between Failure MIIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | CMOS             | Complementary Metal-oxide-semiconductor     |  |
| FP Front Panel FRB Fault Resilient Boot FRU Field Replaceable Unit I'C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAMM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UNB Universal Serial Bus VCCI Voluntary Control Council for Interference  | D2D              | DC-to-DC                                    |  |
| FRB Fault Resilient Boot FRU Field Replaceable Unit IfC Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Serial Bus VCCI Voluntary Control Council for Interference  | EMP              | Emergency Management Port                   |  |
| FRU Field Replaceable Unit If C Inter-integrated Circuit bus LCD Liquid Crystal Display LPC Low-pin Count LSB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended Universal Saynchronous Receiver Transmitter USB Universal Saynchronous Receiver Transmitter USB Universal Saynchronous Receiver Transmitter USB Universal Saynchronous Receiver Transmitter   | FP               | Front Panel                                 |  |
| If C Inter-integrated Circuit bus  LCD Liquid Crystal Display  LPC Low-pin Count  LSB Least Significant Bit  MSB Most Significant Bit  MTBF Mean Time Between Failure  MTTR Mean Time to Repair  NIC Network Interface Card  NMI Non-maskable Interrupt  OTP Over-temperature Protection  OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCI-X Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | FRB              | Fault Resilient Boot                        |  |
| LCD Liquid Crystal Display  LPC Low-pin Count  LSB Least Significant Bit  MSB Most Significant Bit  MTBF Mean Time Between Failure  MTTR Mean Time to Repair  NIC Network Interface Card  NMI Non-maskable Interrupt  OTP Over-temperature Protection  OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCIe* Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | FRU              | Field Replaceable Unit                      |  |
| LPC Low-pin Count  LSB Least Significant Bit  MSB Most Significant Bit  MTBF Mean Time Between Failure  MTTR Mean Time to Repair  NIC Network Interface Card  NMI Non-maskable Interrupt  OTP Over-temperature Protection  OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Serial Bus  VCCI Voluntary Control Council for Interference   | I <sup>2</sup> C | Inter-integrated Circuit bus                |  |
| LESB Least Significant Bit MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Serial Bus VCCI Voluntary Control Council for Interference   | LCD              | Liquid Crystal Display                      |  |
| MSB Most Significant Bit MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | LPC              | Low-pin Count                               |  |
| MTBF Mean Time Between Failure MTTR Mean Time to Repair NIC Network Interface Card NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | LSB              | Least Significant Bit                       |  |
| MTTR Mean Time to Repair  NIC Network Interface Card  NMI Non-maskable Interrupt  OTP Over-temperature Protection  OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCIe* Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Serial Bus  VCCI Voluntary Control Council for Interference   | MSB              | Most Significant Bit                        |  |
| NIC Network Interface Card  NMI Non-maskable Interrupt  OTP Over-temperature Protection  OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCIe* Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | MTBF             | Mean Time Between Failure                   |  |
| NMI Non-maskable Interrupt OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | MTTR             | Mean Time to Repair                         |  |
| OTP Over-temperature Protection OVP Over-voltage Protection PCI Peripheral Component Interconnect PCB Printed Circuit Board PCle* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | NIC              | Network Interface Card                      |  |
| OVP Over-voltage Protection  PCI Peripheral Component Interconnect  PCB Printed Circuit Board  PCIe* Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | NMI              | Non-maskable Interrupt                      |  |
| PCI Peripheral Component Interconnect PCB Printed Circuit Board PCle* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | OTP              | Over-temperature Protection                 |  |
| PCB Printed Circuit Board  PCIe* Peripheral Component Interconnect Express*  PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | OVP              | Over-voltage Protection                     |  |
| PCIe* Peripheral Component Interconnect Express* PCI-X Peripheral Component Interconnect Extended PFC Power Factor Correction POST Power-on Self Test PSU Power Supply Unit RAM Random Access Memory RI Ring Indicate SCA Single Connector Attachment SDR Sensor Data Record SE Single-Ended THD Total Harmonic Distortion UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference   | PCI              | Peripheral Component Interconnect           |  |
| PCI-X Peripheral Component Interconnect Extended  PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | PCB              | Printed Circuit Board                       |  |
| PFC Power Factor Correction  POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | PCIe*            | Peripheral Component Interconnect Express*  |  |
| POST Power-on Self Test  PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | PCI-X            | Peripheral Component Interconnect Extended  |  |
| PSU Power Supply Unit  RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | PFC              | Power Factor Correction                     |  |
| RAM Random Access Memory  RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | POST             | Power-on Self Test                          |  |
| RI Ring Indicate  SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | PSU              | Power Supply Unit                           |  |
| SCA Single Connector Attachment  SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | RAM              | Random Access Memory                        |  |
| SDR Sensor Data Record  SE Single-Ended  THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | RI               | Ring Indicate                               |  |
| SE Single-Ended THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | SCA              | Single Connector Attachment                 |  |
| THD Total Harmonic Distortion  UART Universal Asynchronous Receiver Transmitter  USB Universal Serial Bus  VCCI Voluntary Control Council for Interference   | SDR              | Sensor Data Record                          |  |
| UART Universal Asynchronous Receiver Transmitter USB Universal Serial Bus VCCI Voluntary Control Council for Interference  | SE               | Single-Ended                                |  |
| USB Universal Serial Bus  VCCI Voluntary Control Council for Interference  | THD              | Total Harmonic Distortion                   |  |
| VCCI Voluntary Control Council for Interference  | UART             | Universal Asynchronous Receiver Transmitter |  |
|  | USB              | Universal Serial Bus                        |  |
| VSB Voltage Standby  | VCCI             | Voluntary Control Council for Interference  |  |
|  | VSB              | Voltage Standby                             |  |

### Reference Documents

See the following documents for additional information:

- Intel<sup>®</sup> Server Board S2600IP Technical Product Specification
- Intel<sup>®</sup> Server System R2000IP Product Family Spares/Parts List and Configuration Guide
- Intel<sup>®</sup> Server System R2000IP Service Guide
- Intel<sup>®</sup> Server System R2000IP Quick Installation Guide
- BIOS for EPSD Platforms Based on Intel<sup>®</sup> Xeon Processor E5-4600/2600/2400/1600 Product Families External Product Specification
- EPSD Platforms Based On Intel Xeon® Processor E5 4600/2600/2400/1600 Product Families BMC Core Firmware External Product Specification
- Intel Integrated RAID Module RMS25PB080, RMS25PB040, RMS25CB080, and RMS25CB040 Hardware Users Guide
- Intel<sup>®</sup> Remote Management Module 4 Technical Product Specification
- Intel® Remote Management Module 4 and Integrated BMC Web Console User's Guide